Force mos
Matsuki Electric

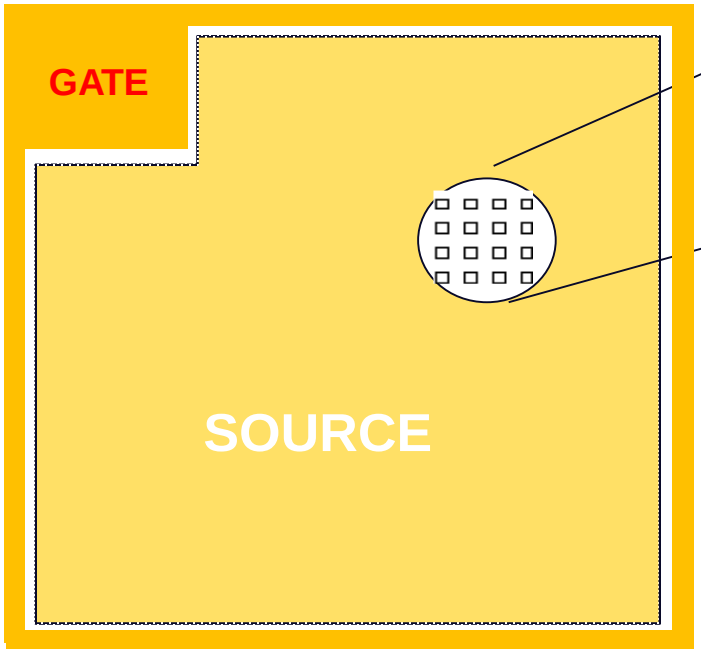
2019 Products
&
Technical MOSFETs

Update:2018.08.13 by Kaoway

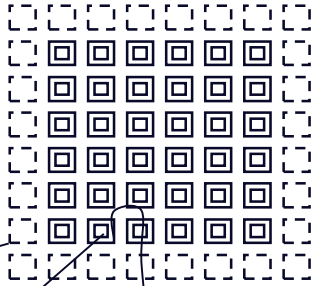
http://www.force-mos.com

MOSFET structure

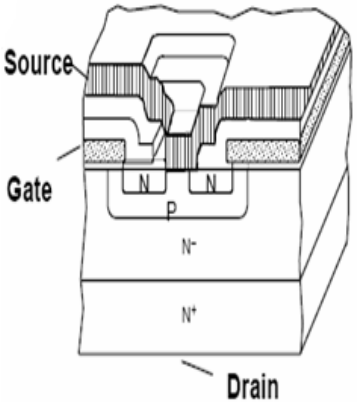
Die top view



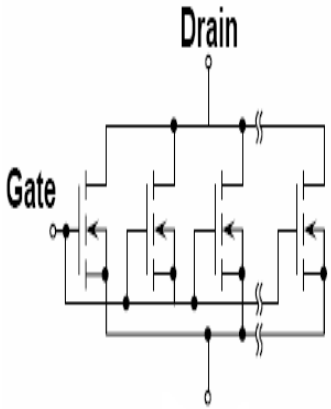
Regional View



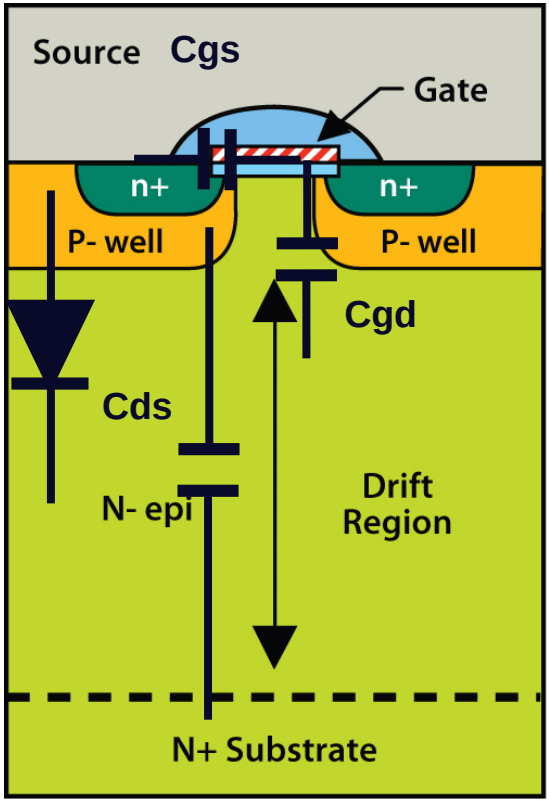
One Cell



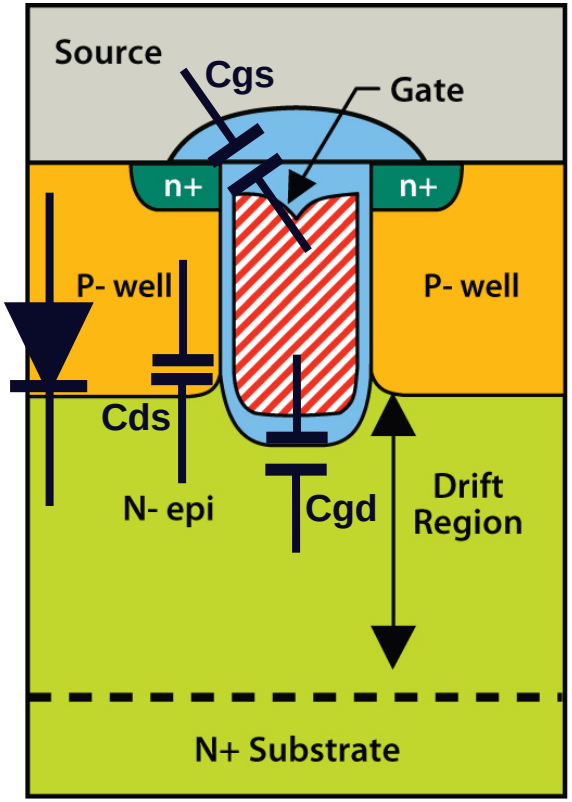
Equivalent ckt



Various power MOSFET Structure

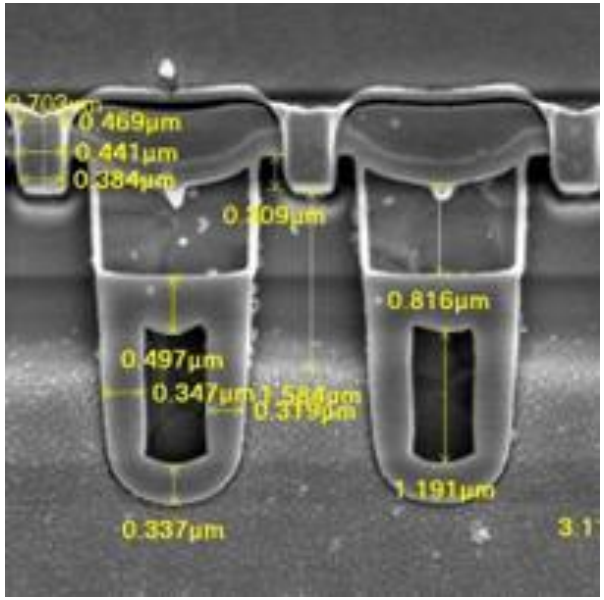


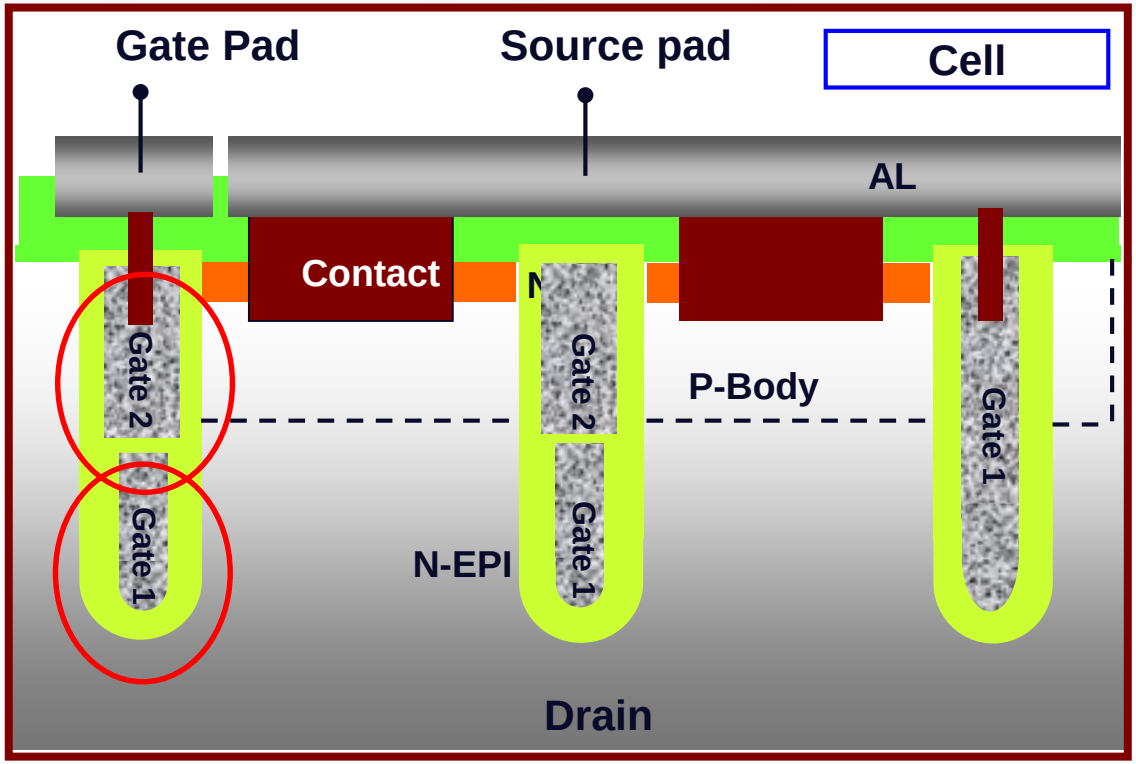
Planar NDMOS



Trench NDMOS

Convention Split gate process

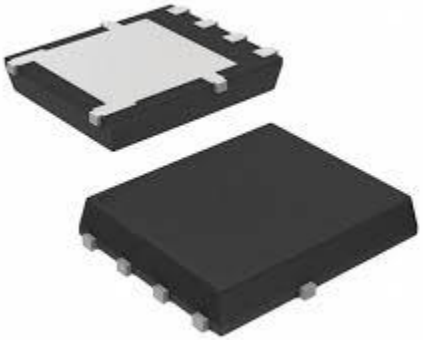




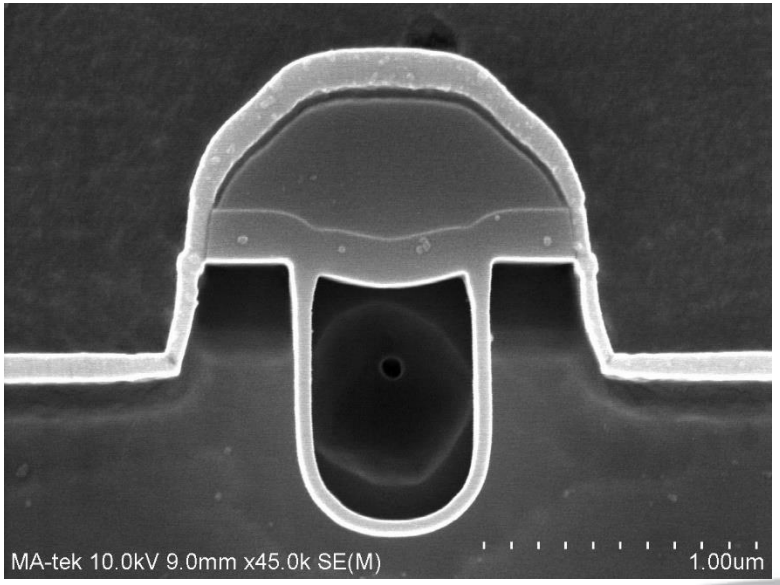
The gate process of Up and down.

Force MOS Technology

- The Patent of three Mask Layer-- LV
- Shielding Gate --- MV
- Super Junction --- HV



Patents For Three Mask Layers



Patent - 1

US008058685B2

(12) **United States Patent**
Hsieh

(10) **Patent No.: US 8,058,685 B2**
(45) **Date of Patent: Nov. 15, 2011**

(54) **TRENCH MOSFET STRUCTURES USING THREE MASKS PROCESS**

(75) Inventor: **Fu-Yuan Hsieh**, Banciao (TW)

(73) Assignee: **Force Mos Technology Co., Ltd.** (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **12/654,327**

(22) Filed: **Dec. 17, 2009**

(65) **Prior Publication Data**

US 2011/0006363 A1 Jan. 13, 2011

Related U.S. Application Data

(63) Continuation-in-part of application No. 12/458,293, filed on Jul. 8, 2009, now Pat. No. 7,816,720.

(51) **Int. Cl.**
H01L 29/772 (2006.01)

(52) **U.S. Cl.** . **257/330**; 257/332; 257/302; 257/E27.091; 257/E29.198; 257/E29.201; 257/E29.26; 257/E21.548; 257/E29.257; 257/E21.55; 257/E21.551; 257/E21.553; 257/E21.655

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

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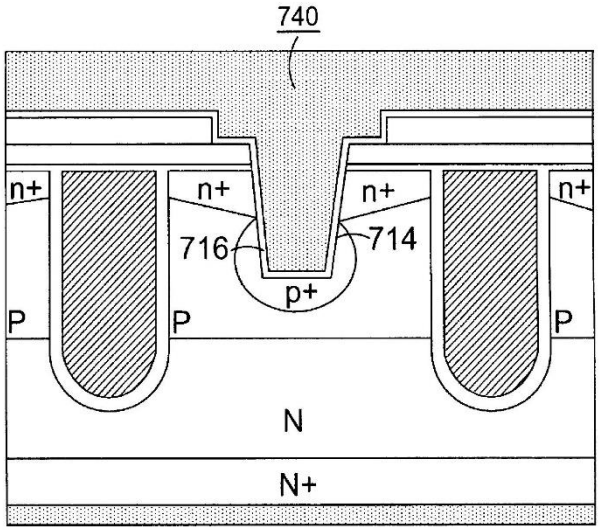
Primary Examiner — Minh-Loan T Tran
Assistant Examiner — Fei Fei Yeung Lopez
(74) *Attorney, Agent, or Firm* — Bacon & Thomas, PLLC

(57) **ABSTRACT**

A trench MOSFET structure having improved avalanche capability is disclosed, wherein the source region is formed by performing source Ion Implantation through contact open region of a contact interlayer, and further diffused to optimize a trade-off between Rds and the avalanche capability. Thus, only three masks are needed in fabrication process, which are trench mask, contact mask and metal mask. Furthermore, said source region has a doping concentration along channel region lower than along contact trench region, and source junction depth along channel region shallower than along contact trench, and source doping profile along surface of epitaxial layer has Guassian-distribution from trenched source-body contact to channel region.

19 Claims, 32 Drawing Sheets



Patent - 2

US008759910B2

(12) **United States Patent**
Hsieh

(10) **Patent No.: US 8,759,910 B2**
(45) **Date of Patent: Jun. 24, 2014**

(54) **TRENCH MOSFET WITH TRENCHED FLOATING GATES HAVING THICK TRENCH BOTTOM OXIDE AS TERMINATION**

(71) Applicant: **Force Mos Technology Co., Ltd.**, New Taipei (TW)

(72) Inventor: **Fu-Yuan Hsieh**, New Taipei (TW)

(73) Assignee: **Force Mos Technology Co., Ltd.**, New Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/953,099**

(22) Filed: **Jul. 29, 2013**

(65) **Prior Publication Data**

US 2013/0307066 A1 Nov. 21, 2013

Related U.S. Application Data

(63) Continuation-in-part of application No. 13/171,965, filed on Jun. 29, 2011, now Pat. No. 8,525,255, which is a continuation-in-part of application No. 12/591,467, filed on Nov. 20, 2009, now Pat. No. 7,989,887.

(51) **Int. Cl.**
H01L 29/78 (2006.01)

(52) **U.S. Cl.**
USPC **257/330**; 257/331; 257/334; 257/315; 257/E29.262; 257/E21.41

(58) **Field of Classification Search**
USPC 257/330, 331, 334, 315, E29.262, 257/E21.41
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

8,525,255 B2 * 9/2013 Hsieh 257/330

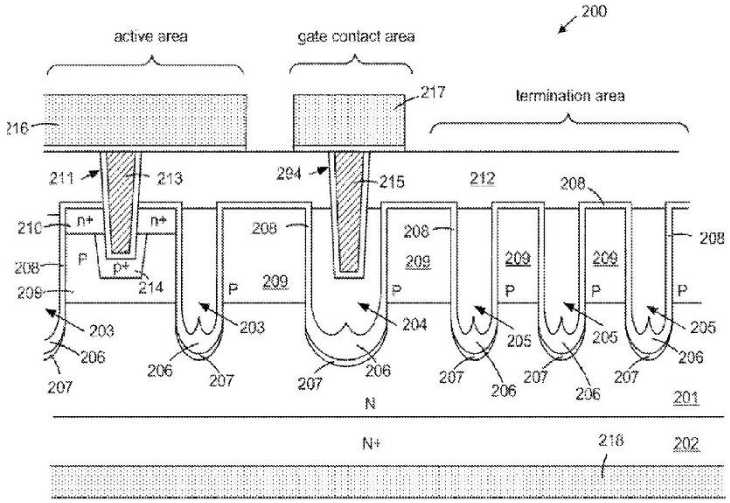
* cited by examiner

Primary Examiner — Long Pham
(74) *Attorney, Agent, or Firm* — Bacon & Thomas, PLLC

(57) **ABSTRACT**

A semiconductor power device with trenched floating gates having thick bottom oxide as termination is disclosed. The gate charge is reduced by forming a HDP oxide layer padded by a thermal oxide layer on trench bottom and a top surface of mesa areas between adjacent trenched gates. Therefore, only three masks are needed to achieve the device structure.

8 Claims, 28 Drawing Sheets



Patent - 3

US008723317B2

(12) **United States Patent**
Hsieh

(10) **Patent No.: US 8,723,317 B2**
(45) **Date of Patent: May 13, 2014**

(54) **TRENCH METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH EMBEDDED SCHOTTKY RECTIFIER USING REDUCED MASKS PROCESS**

(75) Inventor: **Fu-Yuan Hsieh**, New Taipei (TW)

(73) Assignee: **Force Mos Technology Co., Ltd.**, New Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/616,384**

(22) Filed: **Sep. 14, 2012**

(65) **Prior Publication Data**

US 2014/0077290 A1 Mar. 20, 2014

(51) **Int. Cl.**

H01L 23/48	(2006.01)
H01L 23/34	(2006.01)
H01L 23/52	(2006.01)
H01L 21/00	(2006.01)

(52) **U.S. Cl.**
USPC **257/737**; 257/707; 257/751; 438/118

(58) **Field of Classification Search**
USPC 257/330, 302, 332, 737
See application file for complete search history.

(56) **References Cited**

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2011/0278642	A1 *	11/2011	Tu	257/130

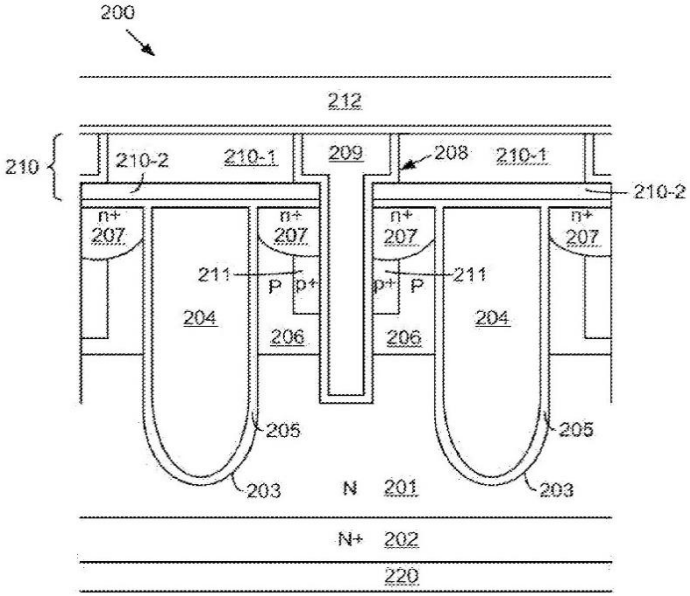
* cited by examiner

Primary Examiner — Long K Tran
Assistant Examiner — Dzung Tran
(74) *Attorney, Agent, or Firm* — Bacon & Thomas, PLLC

(57) **ABSTRACT**

A trench MOSFET with embedded schottky rectifier having at least one anti-punch through implant region using reduced masks process is disclosed for avalanche capability enhancement and cost reduction. The source regions have a higher doping concentration and a greater junction depth along sidewalls of the trenched source-body contacts than along adjacent channel regions near the gate trenches.

11 Claims, 17 Drawing Sheets



Patent - 4

US008530313B2

(12) **United States Patent**
Hsieh

(10) **Patent No.: US 8,530,313 B2**
(45) **Date of Patent: Sep. 10, 2013**

(54) **METHOD OF MANUFACTURING TRENCH MOSFET STRUCTURES USING THREE MASKS PROCESS**

(75) Inventor: **Fu-Yuan Hsieh**, New Taipei (TW)

(73) Assignee: **Force Mos Technology Co., Ltd.** (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/248,479**

(22) Filed: **Sep. 29, 2011**

(65) **Prior Publication Data**

US 2012/0021580 A1 Jan. 26, 2012

Related U.S. Application Data

(60) Division of application No. 12/654,327, filed on Dec. 17, 2009, now Pat. No. 8,058,685, which is a continuation-in-part of application No. 12/458,293, filed on Jul. 8, 2009, now Pat. No. 7,816,720.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.**
USPC **438/270**; 438/268; 438/514; 438/519; 438/527; 438/530; 438/533; 257/E21.41

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

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2013/0001684	A1 *	1/2013	Hsieh	257/334

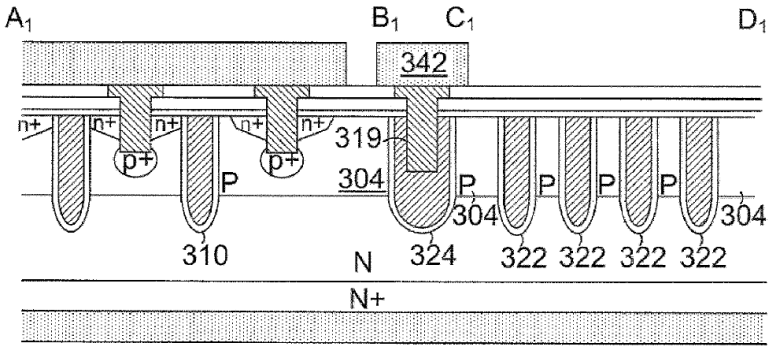
* cited by examiner

Primary Examiner — Fei Fei Yeung Lopez
(74) *Attorney, Agent, or Firm* — Bacon & Thomas, PLLC

(57) **ABSTRACT**

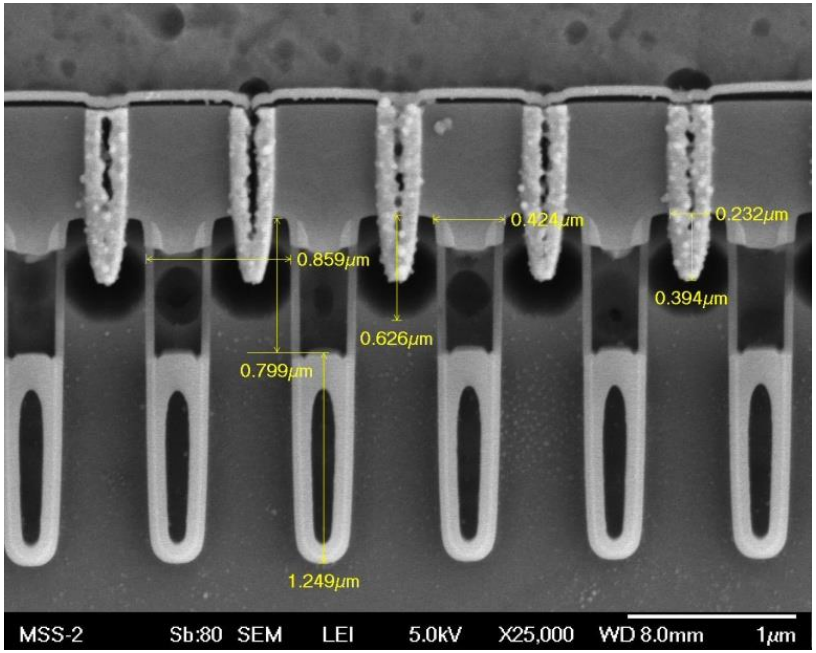
In according with the present invention, a semiconductor device is formed as follows. A contact insulation layer is deposited on the top surface of said silicon layer. A contact mask is applied and following with a dry oxide etching to remove the contact insulation layer from contact open areas. The silicon layer is implanted with a source dopant through the contact open areas and the source dopant is diffused to form source regions, thereby a source mask is saved. A dry silicon etch is carried out to form trenched source-body contacts in the contact open areas, penetrating through the source regions and extending into the body regions.

4 Claims, 32 Drawing Sheets



Force MOS Technology-B

Shielding Gate



Patent

(12) **United States Patent**
Hshieh

(10) **Patent No.: US 8,159,021 B2**
(45) **Date of Patent: Apr. 17, 2012**

(54) **TRENCH MOSFET WITH DOUBLE EPITAXIAL STRUCTURE**

(75) Inventor: **Fwu-Iuan Hshieh**, Saratoga, CA (US)

(73) Assignee: **Force-MOS Technology Corporation** (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 533 days.

(21) Appl. No.: **12/070,853**

(22) Filed: **Feb. 20, 2008**

(65) **Prior Publication Data**

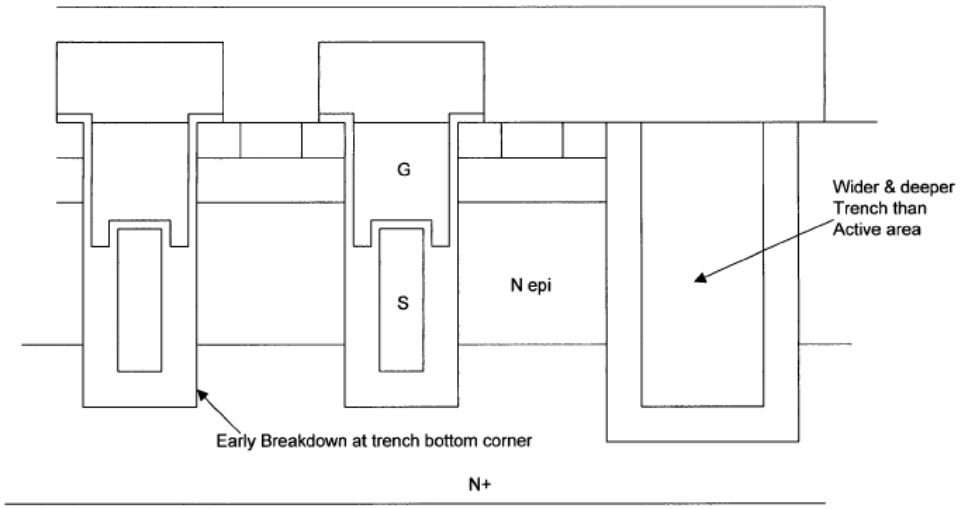


Fig. 1C (Prior Art)

- **Force-MOS own the patent of ETG Process & Structure.**

Performance Benchmark

Normal Trench 60V

EPI		Trench	Gox	P-well		BVDSS	RA45	RA10	VTH	VF11
T	R	um	A	Implant	Drive-in	V	mΩ*cm^2	mΩ*cm^2	V	V
5	0.65	0.9	630	B11, 2.2e12, 30KeV, 7 degree B11, 2.2e12, 140KeV, 7 degree B11, 2.2e12, 300KeV, 7 degree	1000C, 25min	63.03	0.30	0.24	2.12	0.86
	0.7					64.81	0.32	0.26	2.06	0.86
6	0.65					65.13	0.36	0.31	2.00	0.88
	0.7					68.30	0.39	0.34	1.98	0.88

ETG2 60V

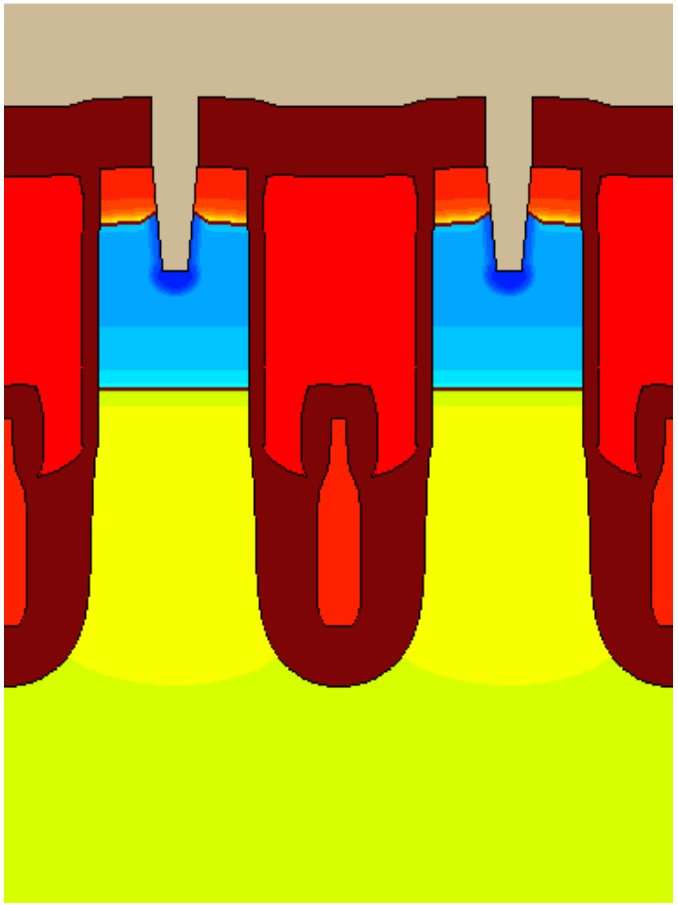
EPI		N-well		P-well		BVDSS	RA45	RA10	VTH	VF11
T	R	Implant	Drive-in	Implant	Drive-in	V	mΩ*cm^2	mΩ*cm^2	V	V
5	0.45	P31, A e13, 140Kev, 0 degree	1150C, 50min	B11, B e13, 40KeV, 0 degree B11, B e13, 140KeV, 0 degree	1000C, 25min	67.260	0.224	0.165	2.126	0.443
	0.55					69.787	0.249	0.188	2.115	0.443
5.5	0.45					68.411	0.246	0.191	1.856	
	0.55					73.622	0.277	0.221	2.055	

Die Shrink 50%

ETG3 60V

EPI		N-well		BOX	Trench	Poly-1	Gox	P-well		BVDSS	RA45	RA10	VTH	VF11	Cell Pitch
T	R	Implant P31, 300keV	Drive-in	um	um	um	A	Implant B11	Drive-in	V	mΩ*cm²	mΩ*cm²	V	V	um
5.3	0.94	1.80E+13	1150C/ 50min	0.3	2.2	0.9	700	1.3e13, 40KeV 1.3e13,180KeV	1000C/ 20min	68	0.24	0.15	2.16	0.40	1.5
		2.20E+13								68	0.21	0.14	1.77	0.41	
5.3	0.94	1.20E+13	1150C/ 50min	0.3	2.2	0.9	700	1.0e13,40KeV 1.0e13,180KeV	1000C/ 20min	68	0.25	0.16	1.80	0.37	1.6
		1.40E+13								68	0.22	0.15	1.60	0.37	
		1.60E+13								69	0.21	0.15	1.63	0.37	

Design Rule Dimension



Cell Pitch: 1.6um

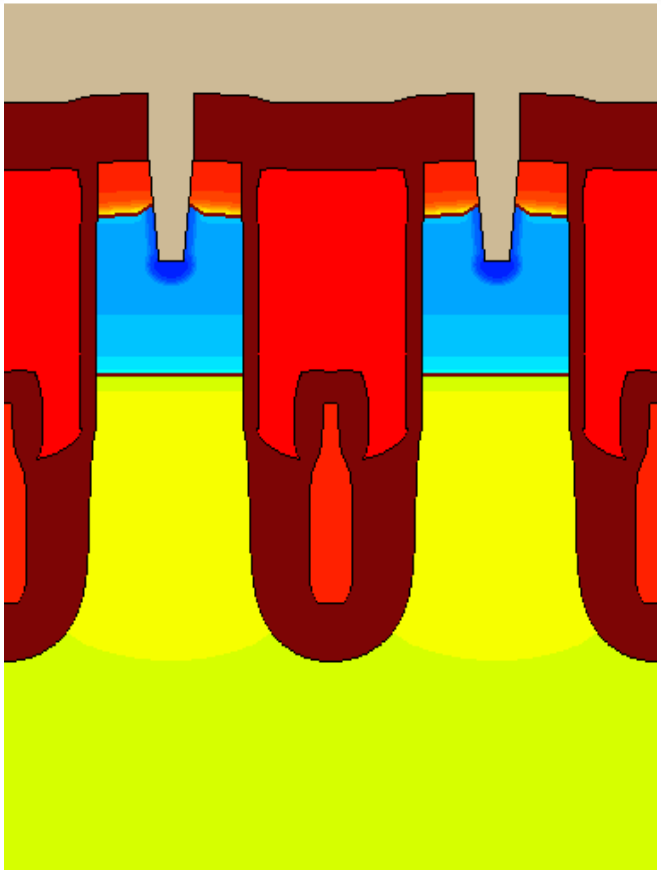
Main Cell:

- Trench Opening: 0.5um
- Contact Opening: 0.24um
- Contact to Trench: 0.43um

Structure:

- Trench Depth: 2.2 um
- Thermal Oxide:0.3um
- Source Poly: 0.9um
- Gate-Oxide: 700A
- Gate Poly : 0.9um
- Contact Recess: 0.4um

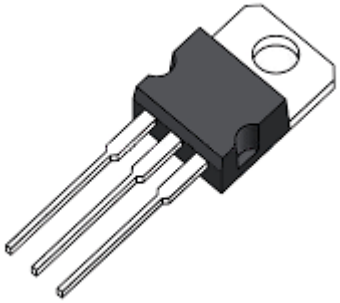
Design Rule Layer



- ✓ N-well
- ✓ Trench
- ✓ Source Poly
- ✓ P-well Mask (Option)
- ✓ Source (N-Plus)
- ✓ Contact
- ✓ Metal

➢ **Total needs 6+1 Layers**

Super Junction HV_MOSFET



Super Junction 600~800V

- **Patent Issue : Expired!**

US005216275A

United States Patent [19]

Chen

[11] **Patent Number: 5,216,275**

[45] **Date of Patent: Jun. 1, 1993**

[54] **SEMICONDUCTOR POWER DEVICES WITH ALTERNATING CONDUCTIVITY TYPE HIGH-VOLTAGE BREAKDOWN REGIONS**

[75] Inventor: **Xingbi Chen**, Sichuan, China

[73] Assignee: **University of Electronic Science and Technology of China**, China

[21] Appl. No.: **761,407**

[22] Filed: **Sep. 17, 1991**

[30] **Foreign Application Priority Data**

Mar. 19, 1991 [CN] China 91101845

[51] **Int. Cl.**[5] **H01L 29/76**; H01L 29/70

[52] **U.S. Cl.** **257/493**; 257/492; 257/287; 257/266; 257/329; 257/655; 257/656

[58] **Field of Search** 357/20, 23.8

[56] **References Cited**

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4,775,881 10/1988 Ploog 357/20

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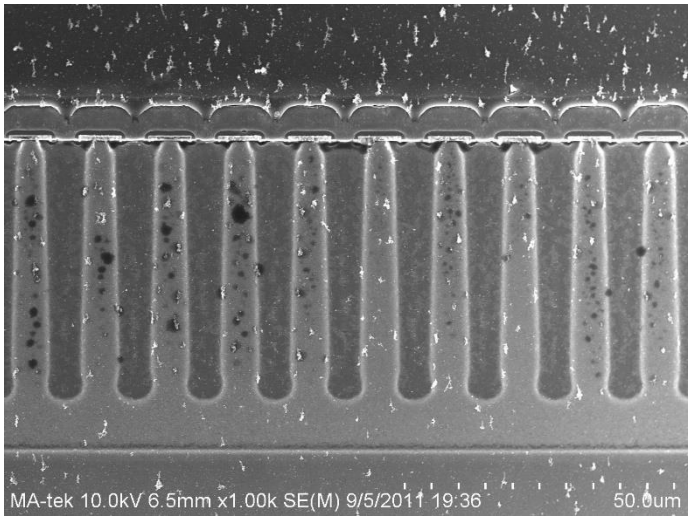
"Self-Aligned MOSFET's with a Specific On-Resistance of . . . ", by Chang et al., IEEE, pp. 2329-2333, 1987.
"Numerical and Experimental Analysis of 500-V Power DMOSFET . . . ,"by Chang et al., IEEE Transactions, vol. 16, NY, Nov. 1989.

Primary Examiner—Jerome Jackson, Jr.
Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

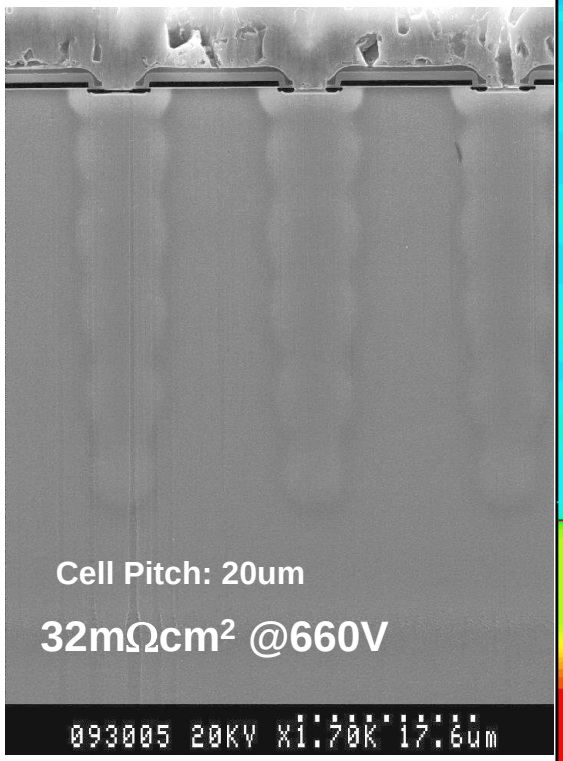
A semiconductor power device wherein the reverse voltage across the p+-regions(s) and the n+-regions(s) is sustained by a composite buffer layer, shortly as CB-layer. The CB-layer contains two kinds of semiconductor regions with opposite types of conduction. These two kinds of regions are alternatively arranged, viewed from any cross-section parallel to the interface between the layer itself and the n+(or p+)-region. Whereas the hitherto-used voltage sustaining layer contains only one kind of semiconductor with single type of conduction in the same sectional view. Design guidelines are also provided in this invention. The relation between the on-resistance in unit area Ron and the breakdown voltage V_B of the CB-layer invented is Ron ocV$_B$[113] which represents a breakthrough to the conventional voltage sustaining layer, whereas the other performances of the power devices remain almost unchanged.

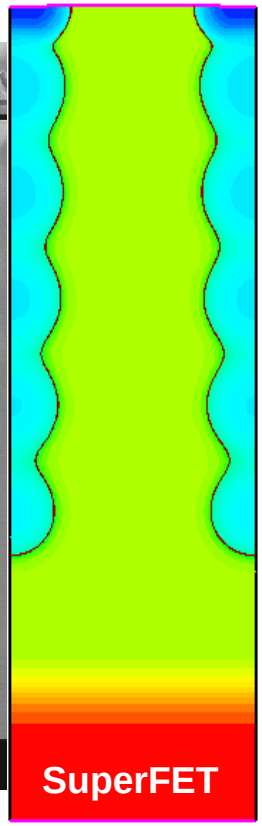
19 Claims, 4 Drawing Sheets

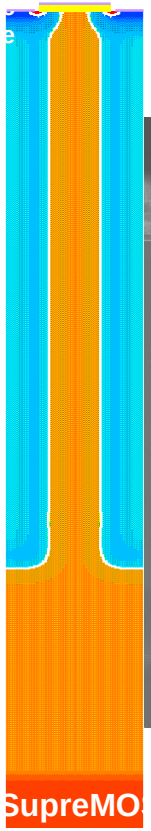


Process introduction

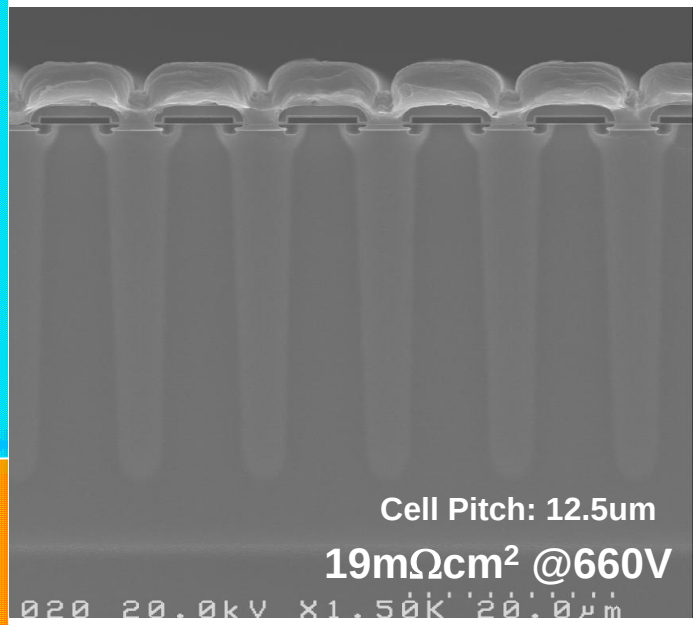
Conventional Multi-Epi Technology





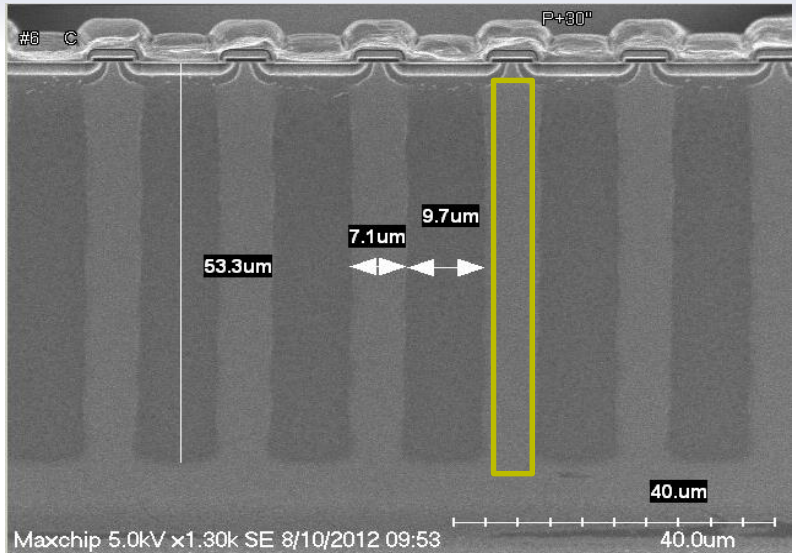


Deep Trench Technology

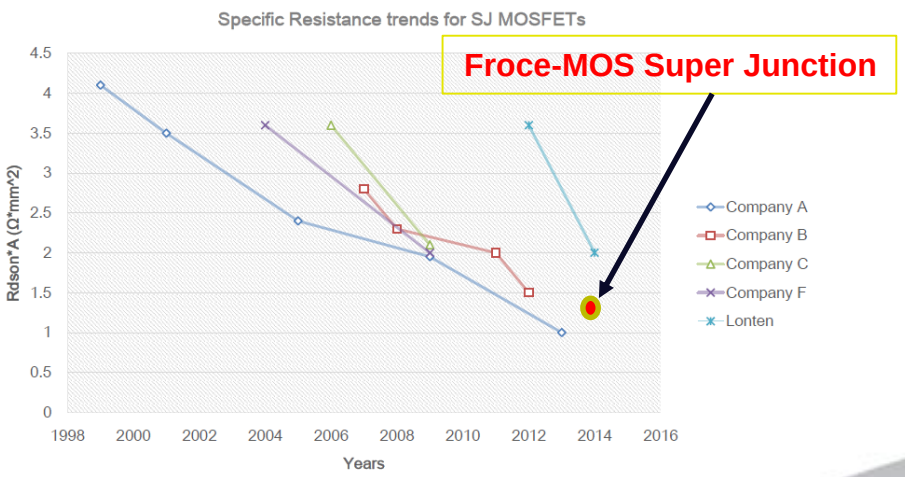


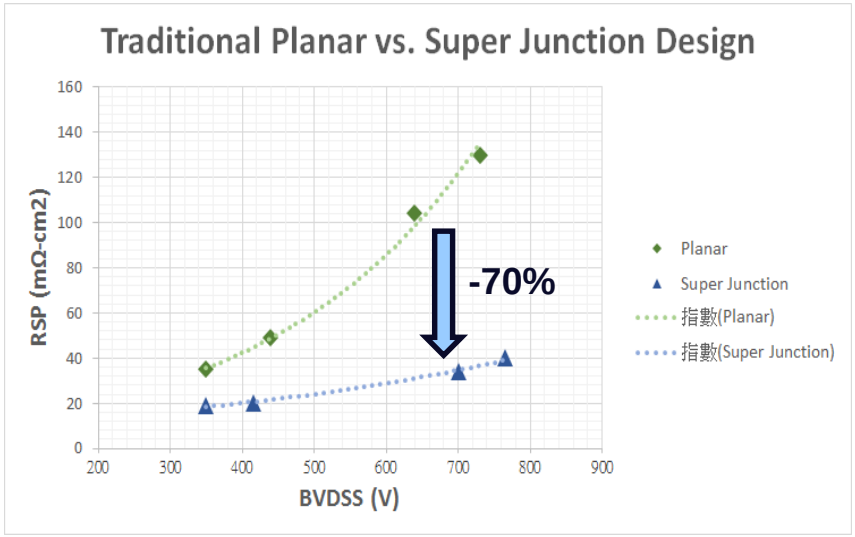
- Higher active cell density
- Stable process parameter during fabrication
- Simple process step
- Special deep trench etching, fill-in process and particle management required

Our New Device



- 用Multi-Epi 做出 Deep Trench的結構特性
- 具有製程較簡單且超低導通電阻的優點
- 台灣第一家高壓Super Junction MOSFET 製造商





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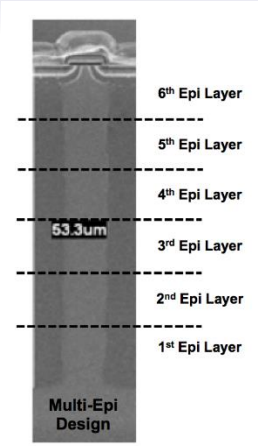
http://www.force-mos.com

Technology Road Map

200V~800V

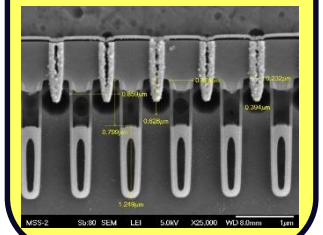
Super Junction



40V~120V

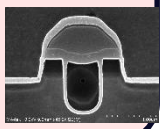
ETG1
Split Gate

ETG2
Shielding Gate



20V~40V

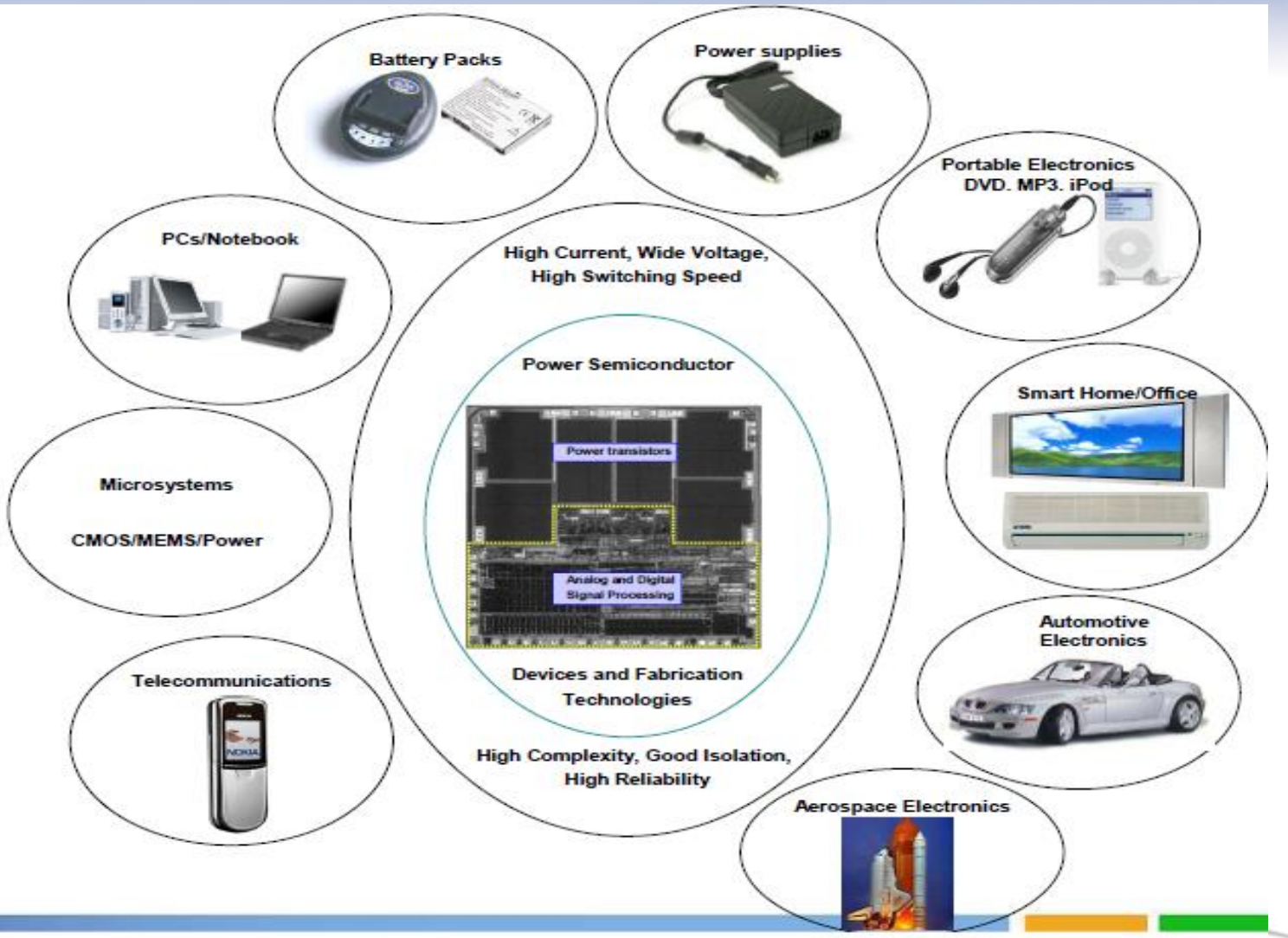
Normal Trench
3 Mask Layer



2018 **2019** **2020** **2021**

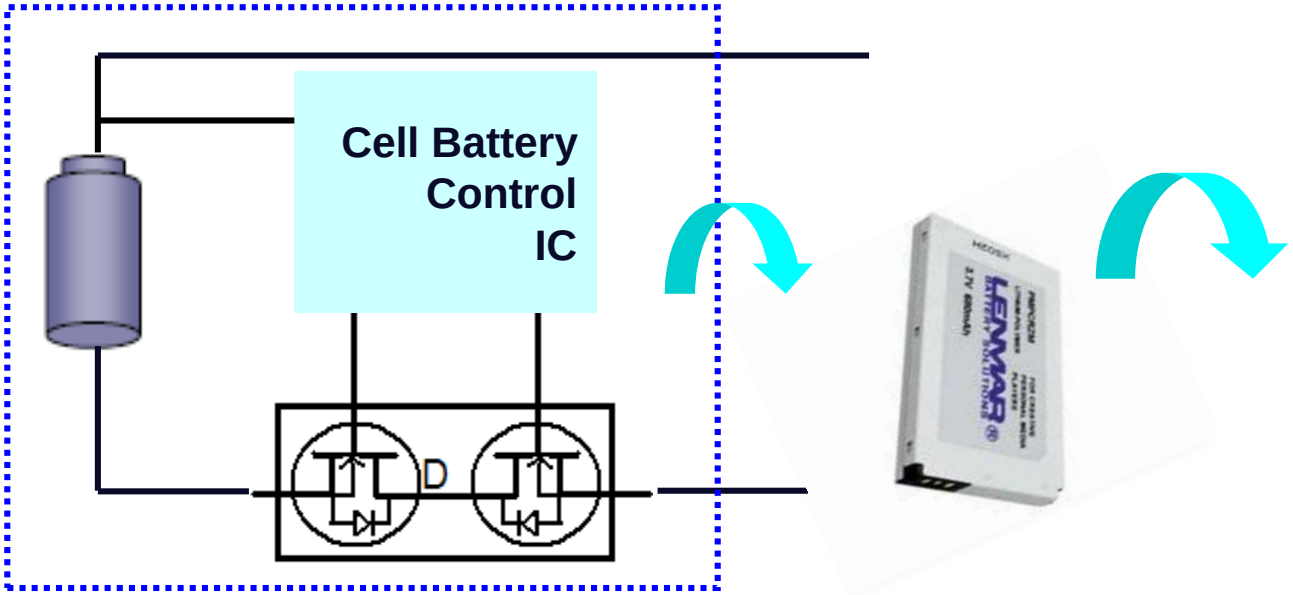
Force mos

MOSFET Product Coverage



Portable Batteries Pack

One/Two cell Battery Packs



Dual N; VDS=20V;ME6968ED(TSOP8)

Dual N; VDS=20V;ME6874DL(DFN3*3)

Dual N; VDS=20V;ME6874(TSOP6)

Single N; VDS=30V;MEE7634(DFN5*6)-FTG

Single N; VDS=20V;ME7620(DFN5*6)-New product

PDA, GPS, MP3, Cell phone and Bluetooth headset reference package design in circuitry.

Customer base

Quanta Computer

Skyworth 创维

wistron

CPT 華中

CHANGHONG

FOXCONN 鴻海科技集團

altek

SHARP

FLEXTRONICS

ITM (주)아이티엠반도체 ITM Semiconductor Co.,LTD

KONKA 康佳

LITEON®

BYD 比亞迪股份有限公司 BYD COMPANY LIMITED

SMP

ECS ELITEGROUP

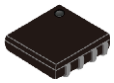
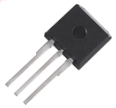
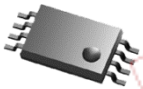
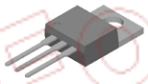
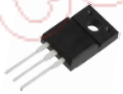
ForceMos Confidential

Supplier

- **Wafer:**

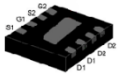
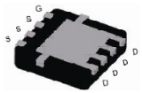
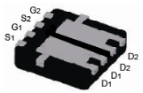
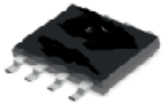
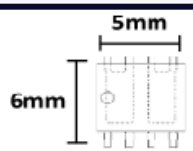
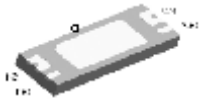
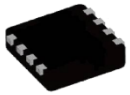
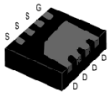
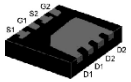
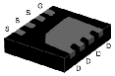
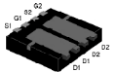
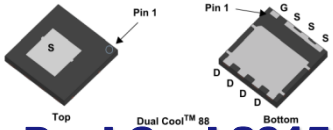
- **Assembly:**

Package Type-1

SOT-23	 J2928-8	SOT-223
TSOP6	TO-251	 SOT-262
SOP-8  TSSOP-8	TO-263	SOT-323 SOT-363
 T0-220  T0-220F	TO-252 3L TO-252 4L	SOT-523 SOT-563
TO-247	SOT-89	SOT-723

ForceMos Confidential

Package Type-2

 DFN2x2 6L DFN2x2 8L	  DFN(S)3.3x3.3 Single DFN(S)3.3x3.3 dual	  LF-PAK56D
DFN3x2	 DFN5x2	
 DFN3x3 NEP	DFN5x6	
  DFN3x3 Single DFN3x3 dual	Power BGA	
  DFN3.3x3.3 Single DFN3.3x3.3 dual	 Dual Cool 2015	

MOSFET Application products

ID(A)

>50A

30A

10A

Server
ME7686/ME7636/ME7170

PC
ME60N03A(S)
ME70N03A(S)
ME20N03
ME7686/ME7386(PPAK)

DC Module
ME7686/ME7636
ME7686/ME7358(9)
ME80N08

Power Tool
ME60N06
ME7640 RDS_on <1m ohm
ME7644 RDS_on <0.9m ohm

NB
ME7686/7636(PPAK)
ME7686/7170(PPAK)
ME4856/ME4626
ME4384
ME4410A/B
ME4920….

Battery
ME8018, ME8017
ME4626, ME8027

E-Bike
ME75N80
ME80N08
ME100N15T

Versatility-Package, HV Tech, Reliability

Inverter

ME4542/ME3948/ME3500/ME4565D4
/ME60N04/ME70P04/ME4946

Consumer
ME2320D
ME2323D
ME1403D
ME8803D

DC-FAN
ME2306/ME4542ME4946

DSC flash (IGBT)

LED lighting(ME23XX)

20V 30V 40V 60V 80~200V 500V

Force mos
Matsuki Electric

Thank You

http://www.force-mos.com