

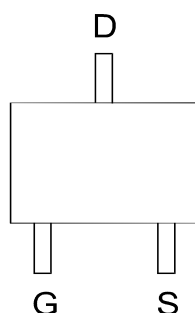
GENERAL DESCRIPTION

The ME2N70022D2W-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(SOT-323)

Top View

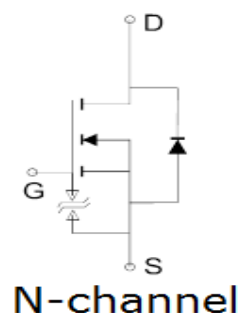


FEATURES

- $R_{DS(ON)} \leq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=4.5V$
- ESD Protection HBM >2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



Ordering Information: ME2N70022D2W-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain	$T_A=25^\circ\text{C}$	I_D	0.27	A
	$T_A=70^\circ\text{C}$	I_D	0.21	
Pulsed Drain Current		I_{DM}	1.07	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	0.34	W
	$T_A=70^\circ\text{C}$	P_D	0.22	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	367	$^\circ\text{C/W}$

* The device mounted on 1in² FR4 board with 2 oz copper

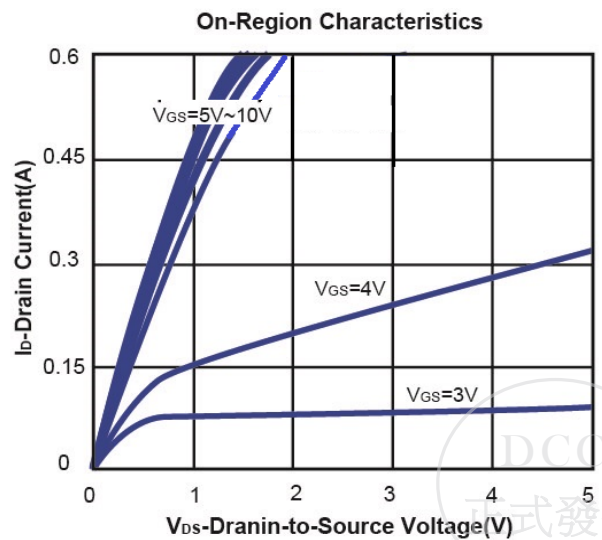
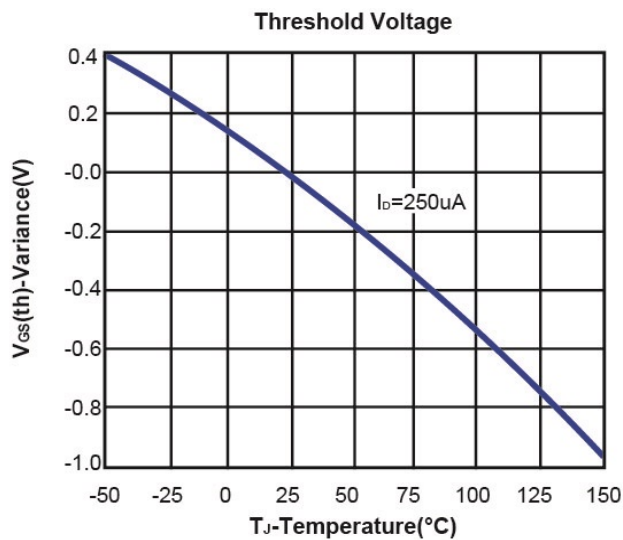
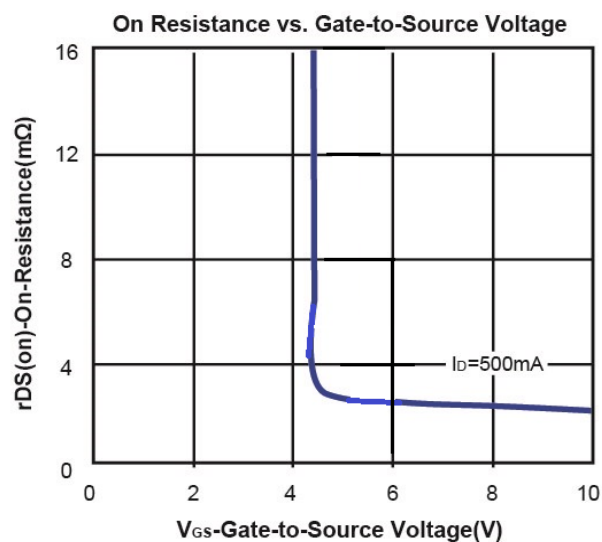
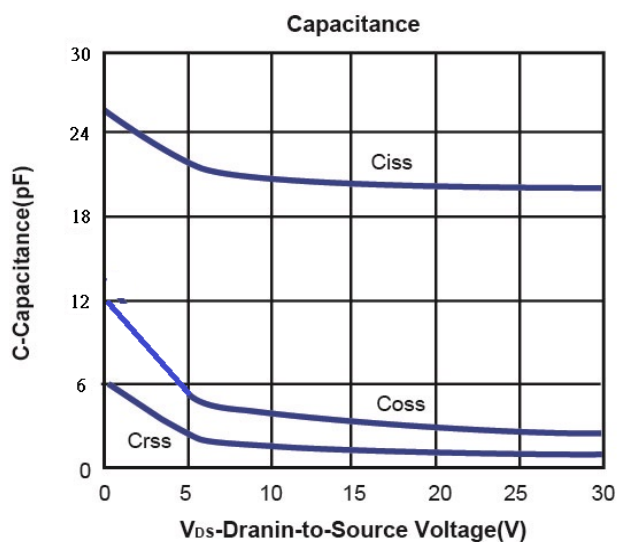
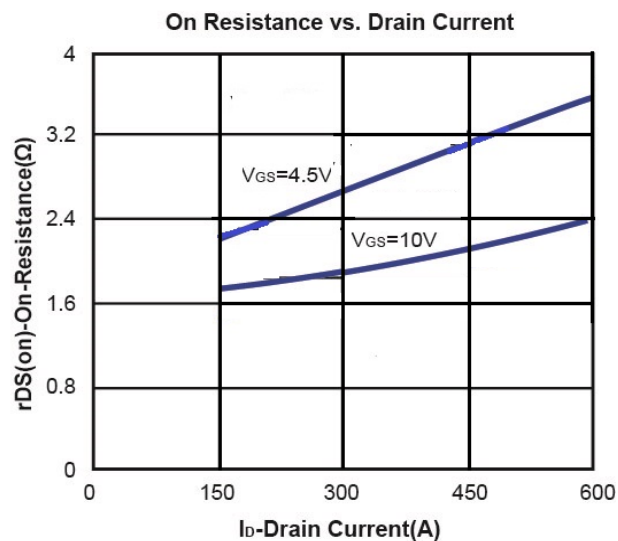
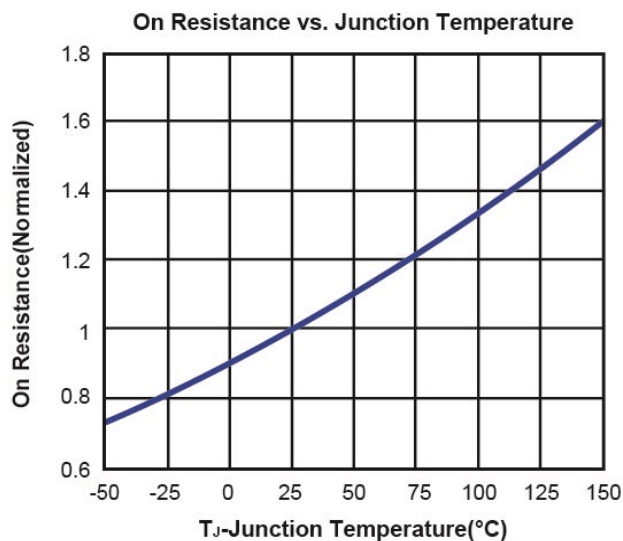
Electrical Characteristics (TA=25℃ Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0, I _D =10uA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.3		2.1	V
I _{GSS}	Gate Body Leakage	V _{GS} = ±20V, V _{DS} =0V			±10	uA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	uA
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =500mA			3	Ω
		V _{GS} =4.5V, I _D =200mA			4	
V _{SD}	Diode Forward Voltage	I _S =200mA, V _{GS} =0V			1.2	V
Dynamic						
Qg	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =200mA		3.7		nC
Qg	Total Gate Charge	V _{DS} =30V, V _{GS} =4.5V, I _D =200mA		1.4		
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			0.2		
Ciss	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		21		pF
Coss	Output Capacitance			3		
Crss	Reverse Transfer Capacitance			1		
t _{d(on)}	Turn-On Delay Time	V _{DS} =30V, R _L =150Ω V _{GS} =10V, R _{GS} =10Ω I _D =200mA		3.5		Ns
t _r	Turn-On Rise Time			20.3		
t _{d(off)}	Turn-Off Delay Time			4.4		
t _f	Turn-Off Fall Time			22.2		

Notes : a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

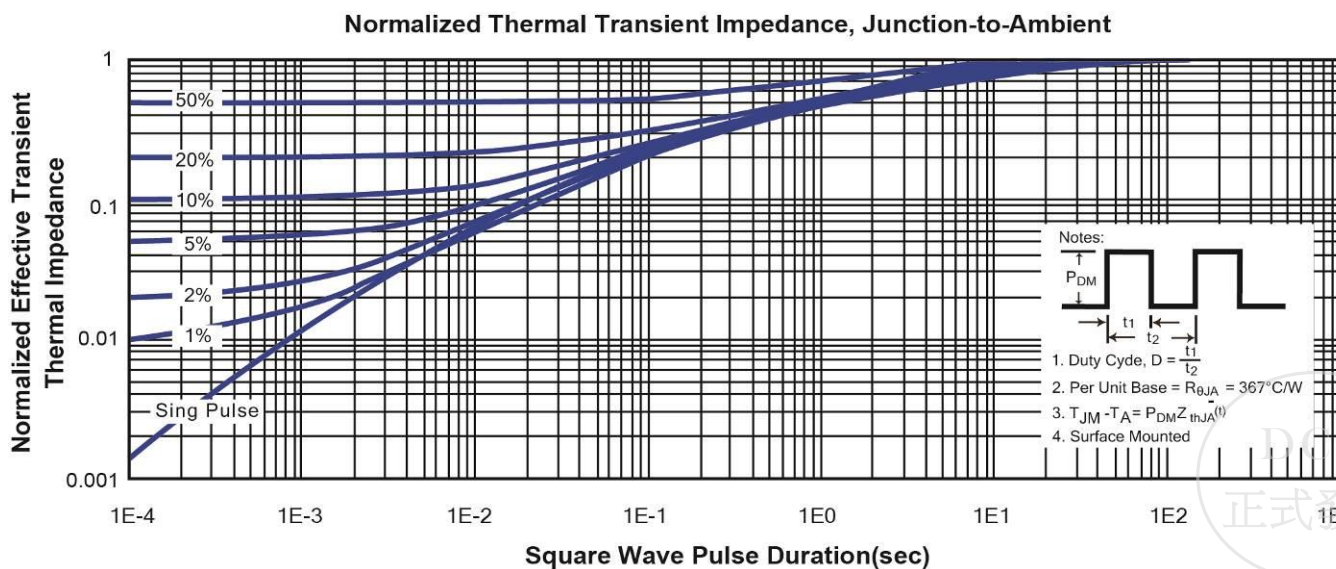
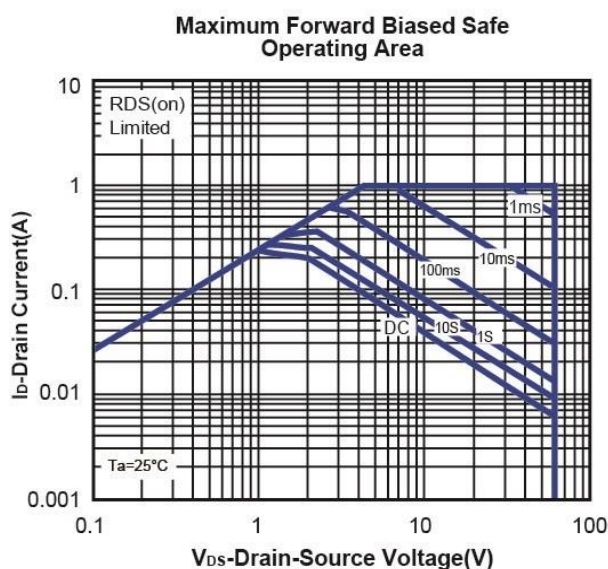
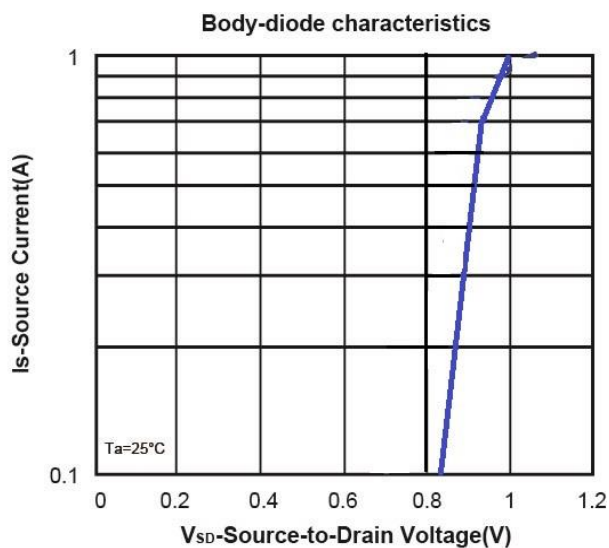
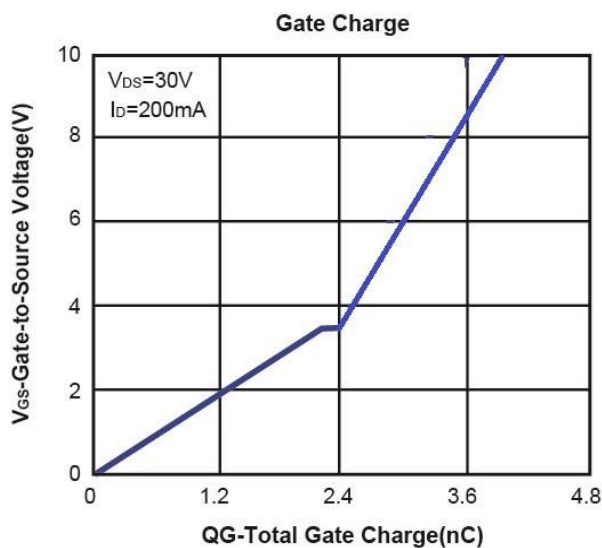
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



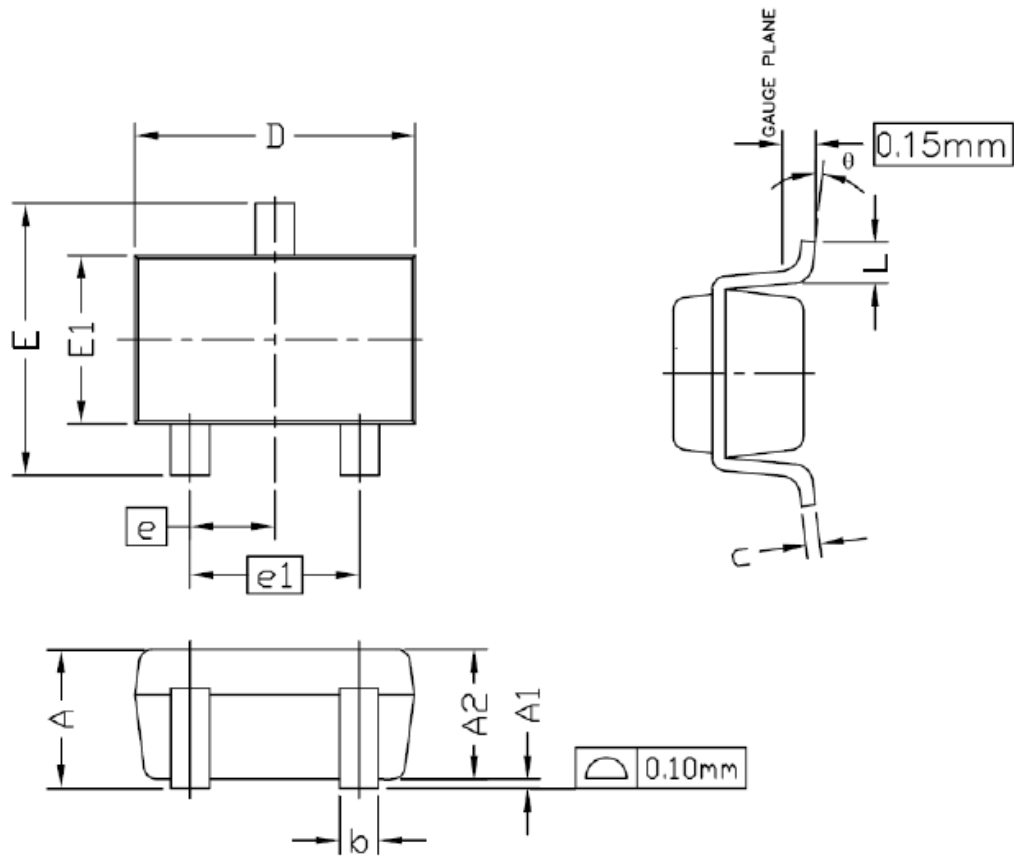


N-Channel 60-V(D-S) MOSFET – ESD Protected

Typical Characteristics (T_J =25°C Noted)



SOT-323 Package Outline

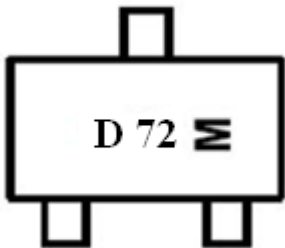


SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.20	0.40
c	0.08	0.22
D	1.80	2.20
E	1.80	2.45
e	0.65 BSC	
e1	1.30 BSC	
E1	1.10	1.40
L	0.20	0.46
θ	0°	8°



Package: SOT-323

Marking Code:



D72: Device Marking Code
M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

