ME2N70022E1W-G(Green)

N-Channel 60-V(D-S) MOSFET – ESD Protected

GENERAL DESCRIPTION

The ME2N70022E1W-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 4\Omega$@V_{GS}=10V
- $R_{DS(ON)} \leqq 4\Omega$@V_{GS}=5V
- ESD Protection HBM >1KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

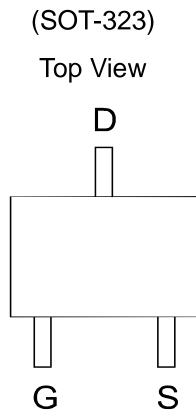
APPLICATIONS

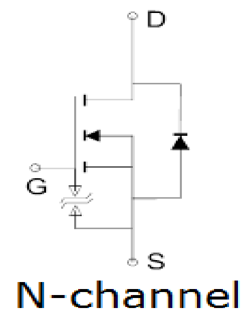
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-323)

Top View





Ordering Information: ME2N70022E1W-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.23	A
	T_A=70℃	I_D	0.18	
Pulsed Drain Current		I_{DM}	0.92	A
Maximum Power Dissipation	T_A=25℃	P_D	0.34	W
	T_A=70℃	P_D	0.22	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	367	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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N-Channel 60-V(D-S) MOSFET – ESD Protected

Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

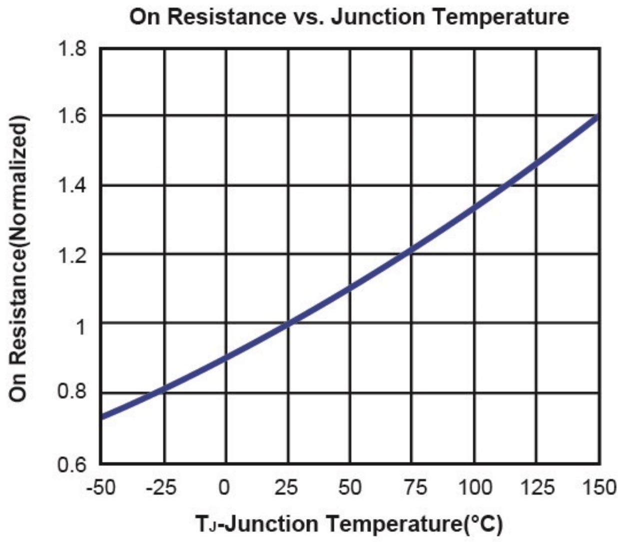
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=10uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1		2	V
I_{GSS}	Gate Body Leakage	V_{GS}= ±20V , V_{DS}=0V			±1	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	uA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=500mA			4	Ω
		V_{GS}=5V, I_D=50mA			4	
V_{SD}	Diode Forward Voltage	I_S=200mA, V_{GS}=0V			1.2	V
Dynamic						
Qg	Total Gate Charge	VDS=30V,VGS=10V,ID=200mA		3.7		nC
Qg	Total Gate Charge	VDS=30V,VGS=4.5V,ID=200mA		1.4		
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			0.2		
Ciss	Input Capacitance	VDS=25V, VGS=0V, f=1MHz		21		pF
Coss	Output Capacitance			3		
Crss	Reverse Transfer Capacitance			1		
$t_{d(on)}$	Turn-On Delay Time	VDS=30V, RL =150Ω VGS=10V,RGS=10Ω ID=200mA		3.5		Ns
t_r	Turn-On Rise Time			20.3		
$t_{d(off)}$	Turn-Off Delay Time			4.4		
t_f	Turn-Off Fall Time			22.2		

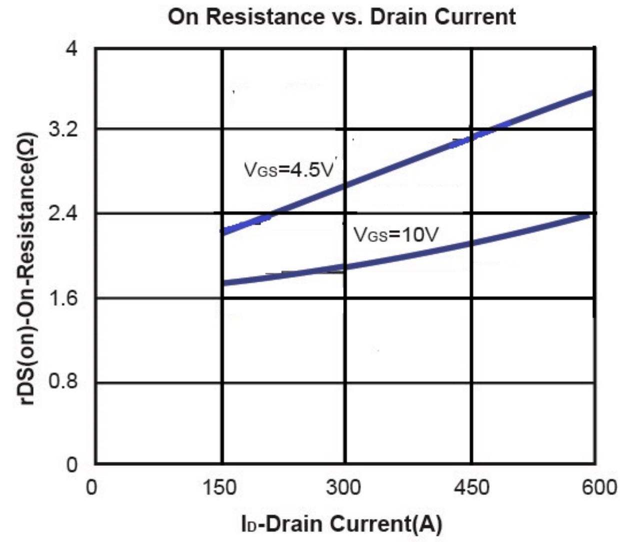
Notes：a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

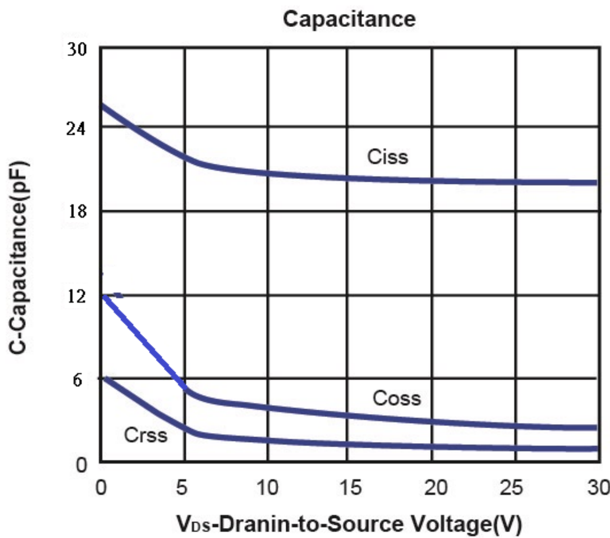
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

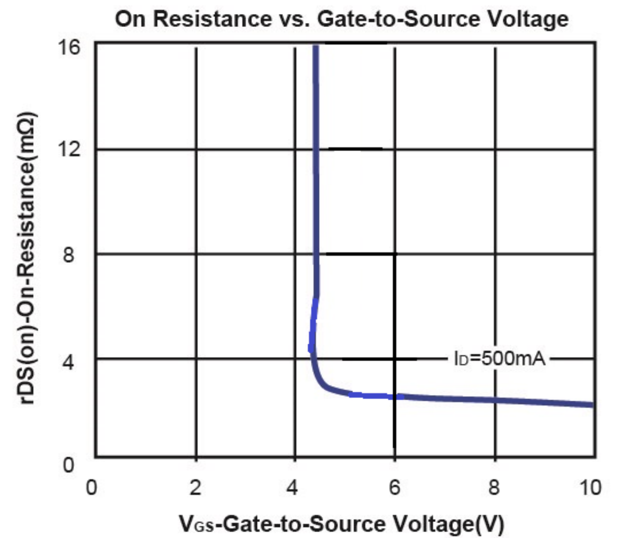
N-Channel 60-V(D-S) MOSFET – ESD Protected

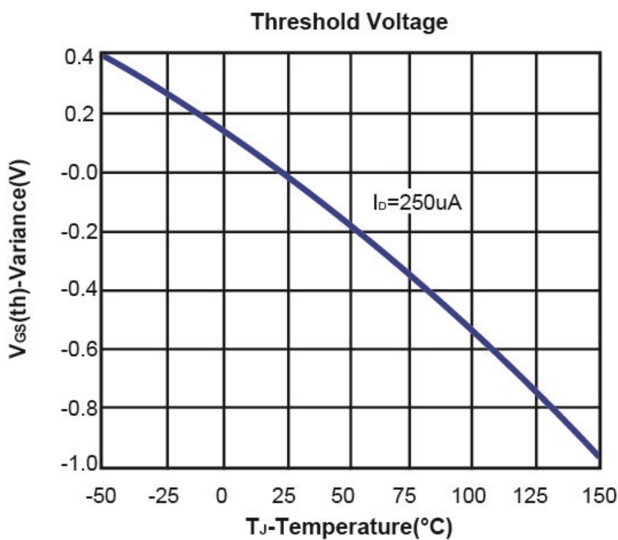
Typical Characteristics (TJ =25℃ Noted)

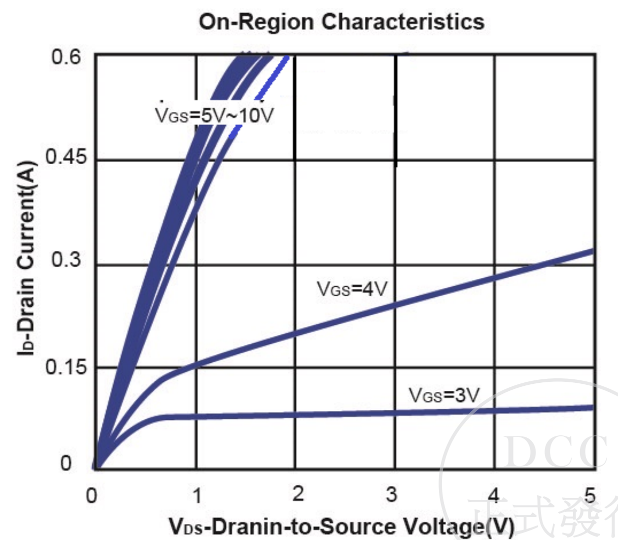












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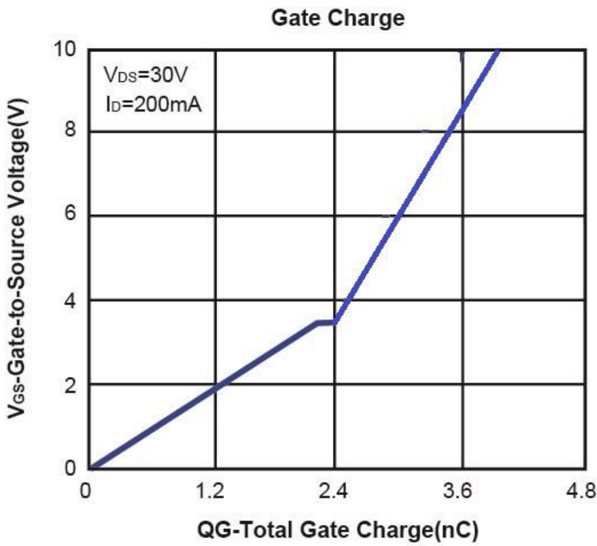
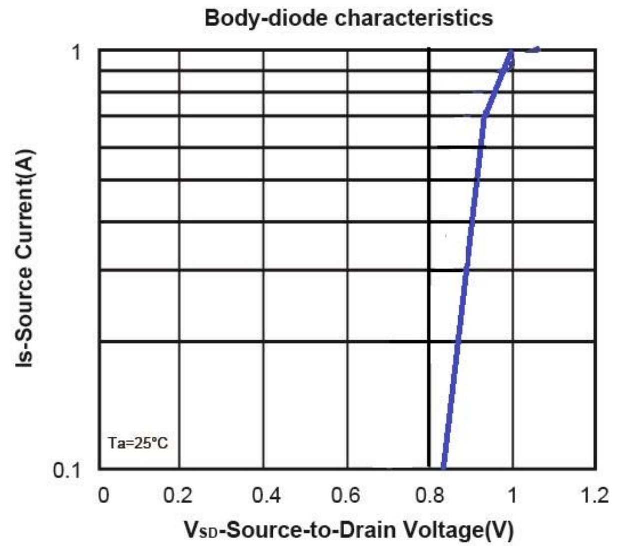
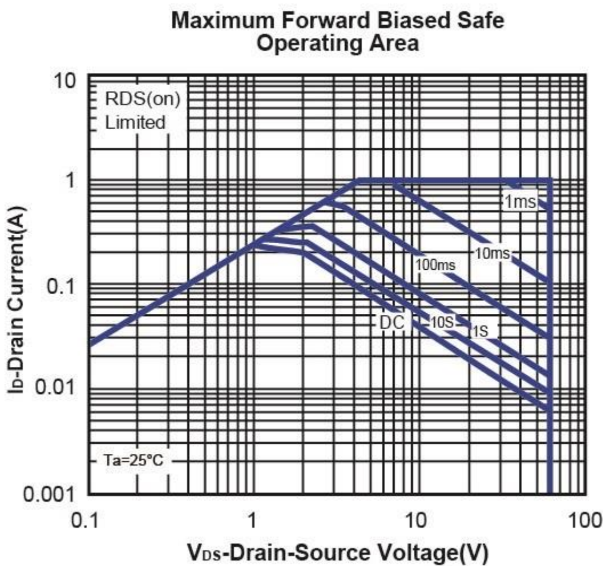
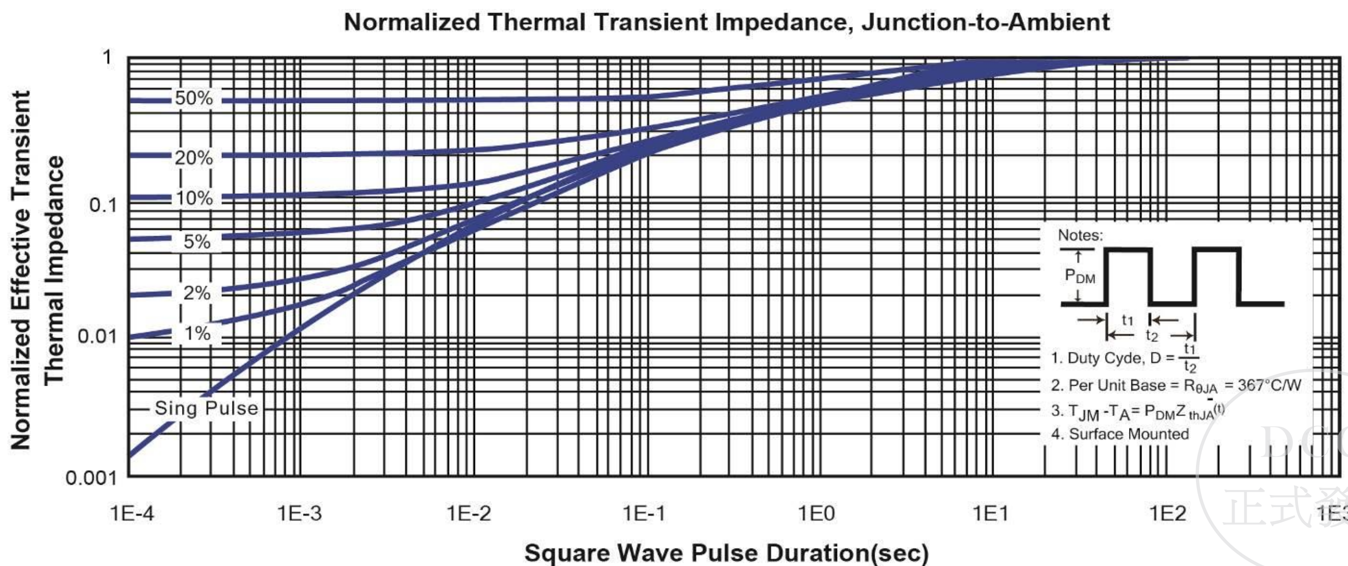
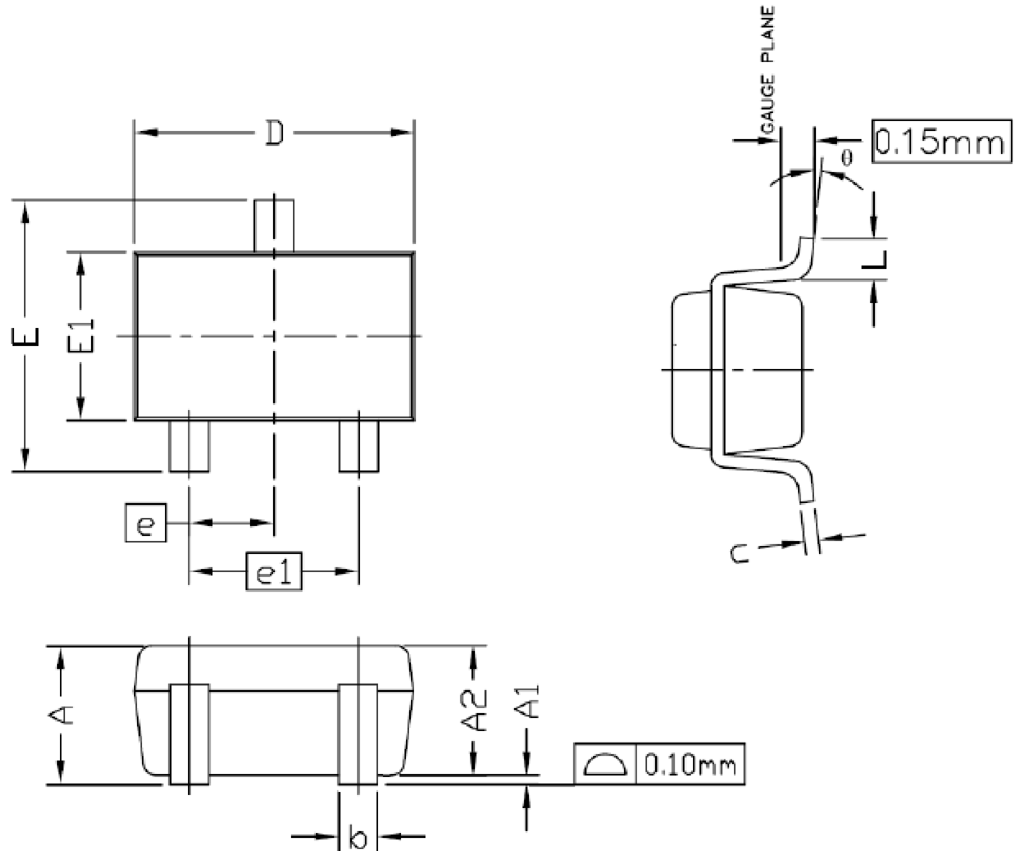








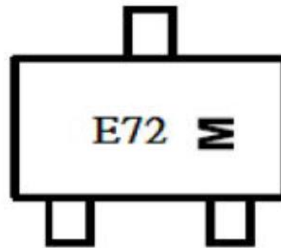
SOT-323 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.20	0.40
c	0.08	0.22
D	1.80	2.20
E	1.80	2.45
e	0.65 BSC	
e1	1.30 BSC	
E1	1.10	1.40
L	0.20	0.46
θ	0°	8°

Package: SOT-323

Marking Code:



E72: Device Marking Code
M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

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