N-Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N7002DL-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦2.8Ω@V_{GS}=10V
- $R_{DS(ON)}$ ≦3.8Ω@V_{GS}=4.5V
- ESD Protection HBM≧2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

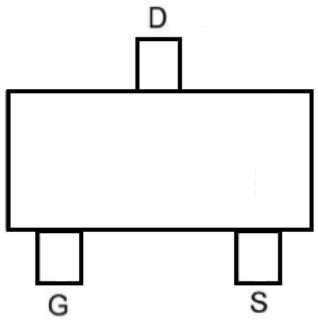
APPLICATIONS

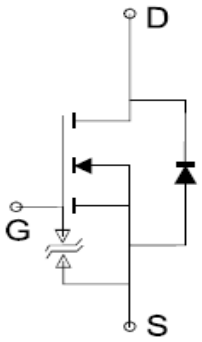
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

Small SOT-23

Top View





N-Channel MOSFET

Ordering Information: ME2N7002DL-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.30	A
	T_A=70℃	I_D	0.24	
Pulsed Drain Current		I_{DM}	2	A
Maximum Power Dissipation	T_A=25℃	P_D	0.35	W
	T_A=70℃	P_D	0.21	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	℃/W
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	106	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA		1.9	2.8	Ω
		V_{GS}=4.5V, I_D=200mA		2.4	3.8	
V_{SD}	Diode Forward Voltage	I_S=200mA, V_{GS}=0V		0.7	1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=10V,I_D=200mA		5.01		nC
Qgs	Gate-Source Charge			2.58		
Qgd	Gate-Drain Charge			1.25		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		13		pF
Coss	Output Capacitance			2.62		
Crss	Reverse Transfer Capacitance			1.76		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, R_L =150Ω V_{GS}=4.5V,R_G=10Ω I_D=200mA		3.5		ns
t_r	Turn-On Rise Time			19.4		
$t_{d(off)}$	Turn-Off Delay Time			17.9		
t_f	Turn-Off Fall Time			22.5		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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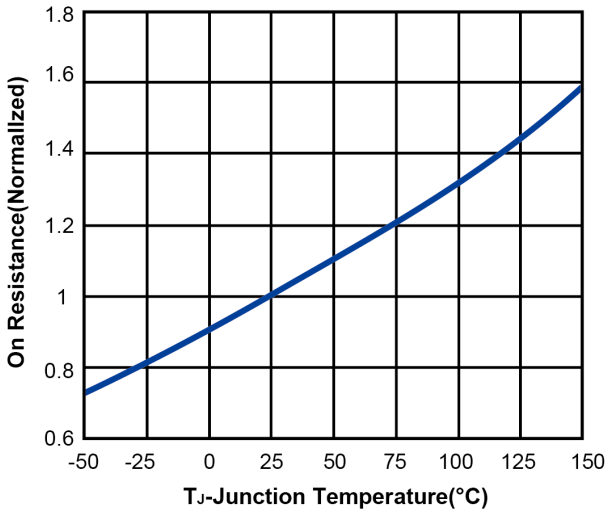
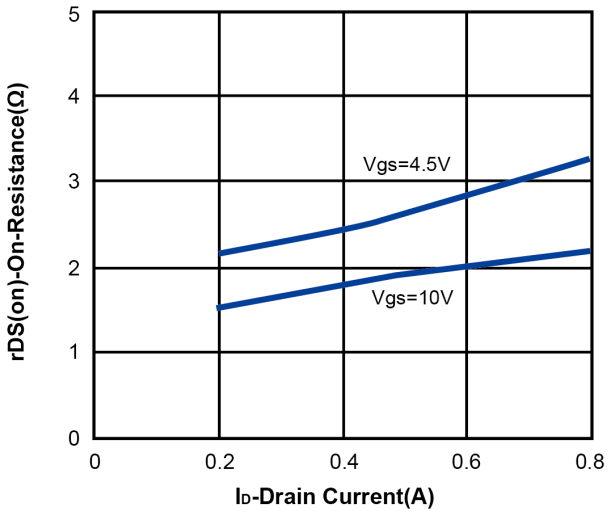
Typical Characteristics (T_J =25℃ Noted)

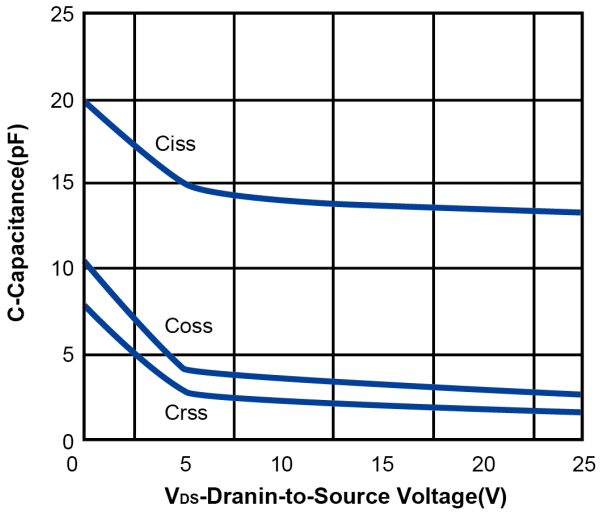
On Resistance vs. Junction Temperature



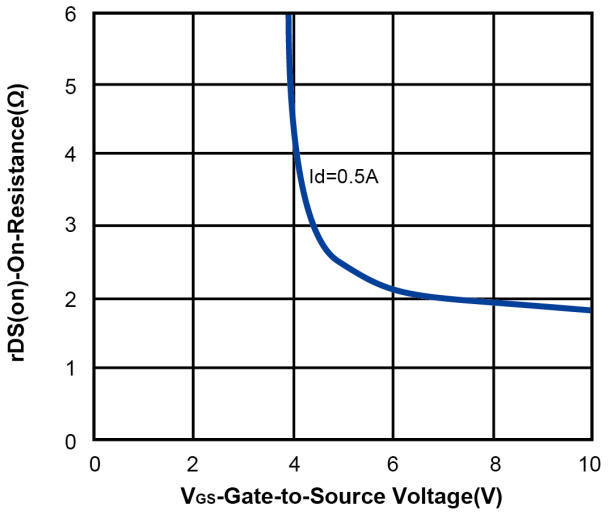
On Resistance vs. Drain Current



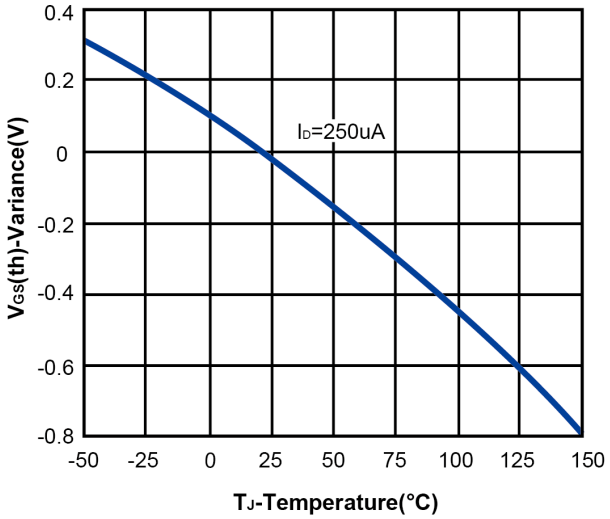
Capacitance



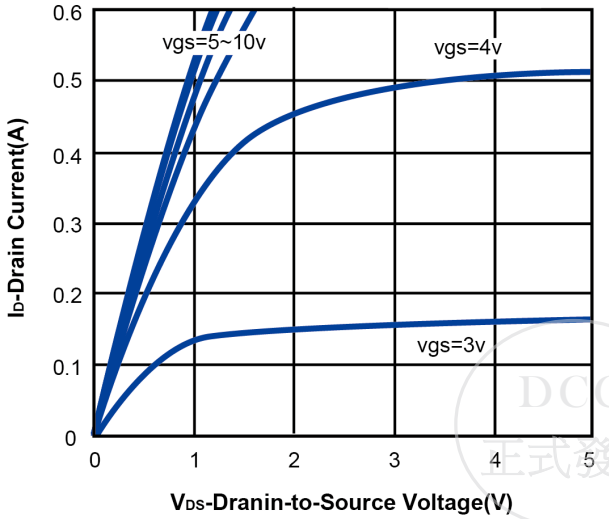
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

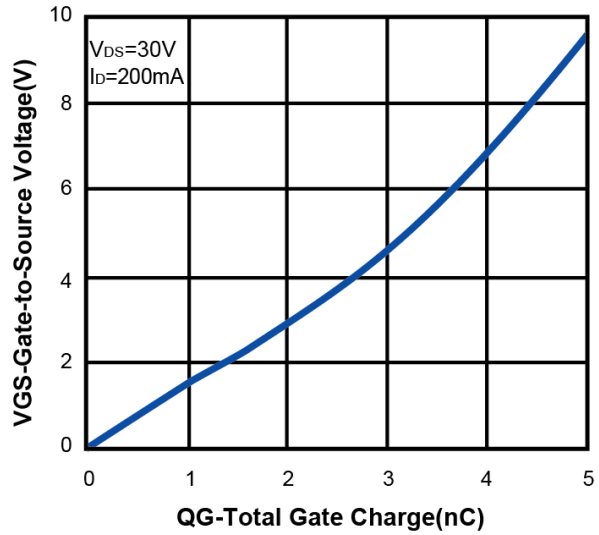


On-Region Characteristics

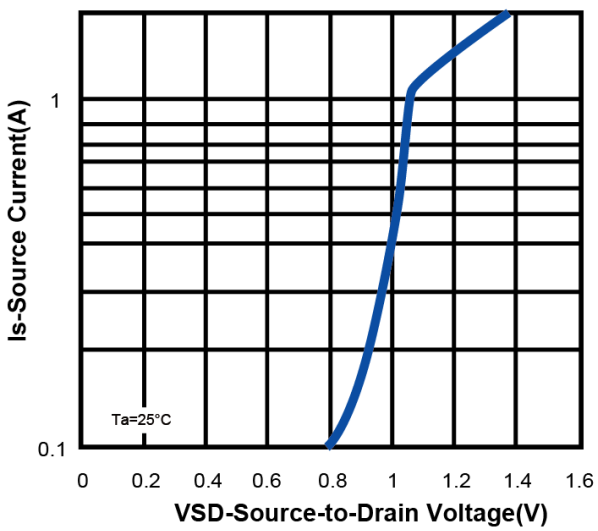


N-Channel 60V (D-S) MOSFET, ESD Protection
Typical Characteristics (T_J =25℃ Noted)

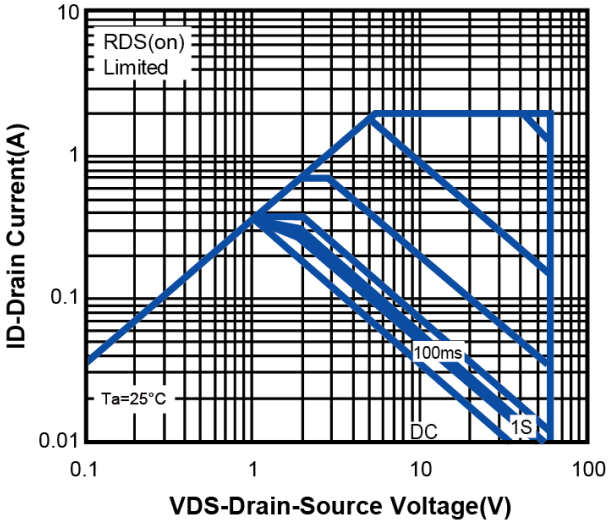
Gate Charge



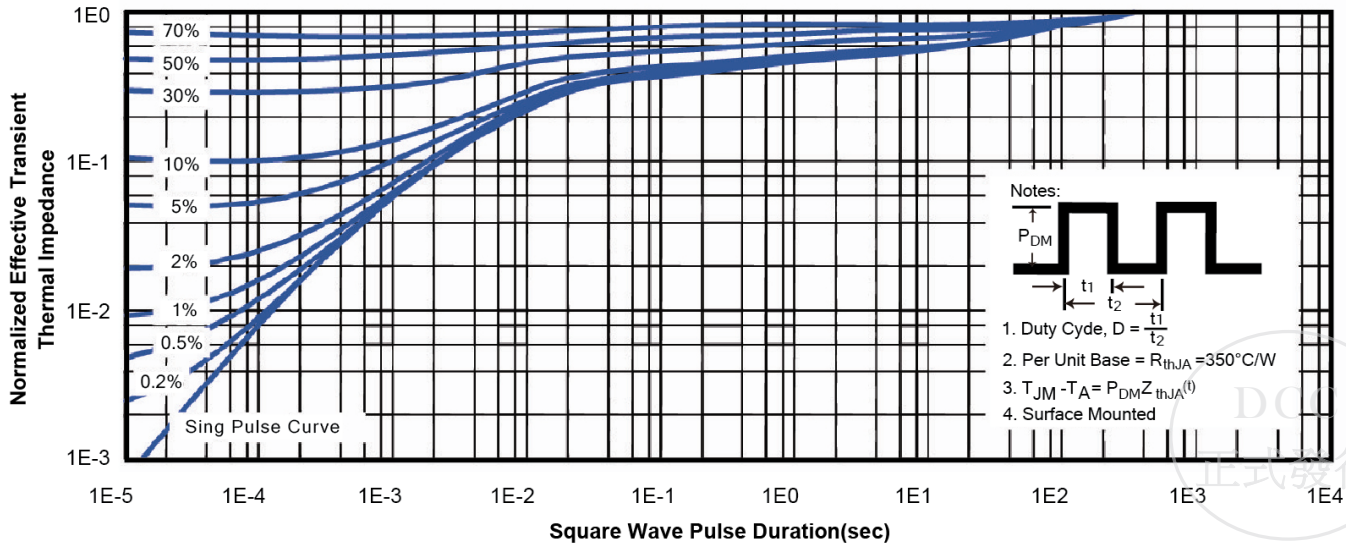
Body-diode characteristics



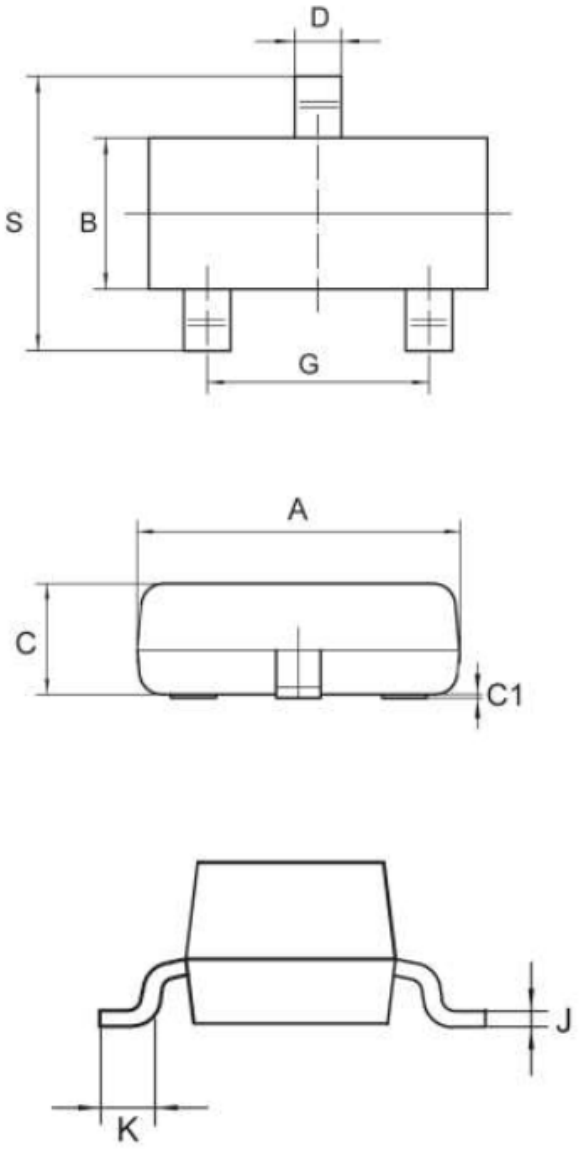
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Small SOT-23 Package



Symbol	MILLIMETERS	
	MIN	MAX
A	2.8	3.0
B	1.2	1.4
C	0.9	1.1
C1	-	0.1
D	0.3	0.5
G	1.90 REF	
J	0.05	0.15
K	0.2	-
S	2.2	2.6