N-Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N7002DN-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

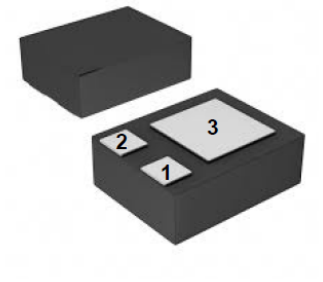
FEATURES

- $R_{DS(ON)}$ ≦2.8Ω@V_{GS}=10V
- $R_{DS(ON)}$ ≦3.7Ω@V_{GS}=4.5V
- $R_{DS(ON)}$ ≦4.4Ω@V_{GS}=3V
- ESD Protection HBM≧2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding
- MSL1

APPLICATIONS

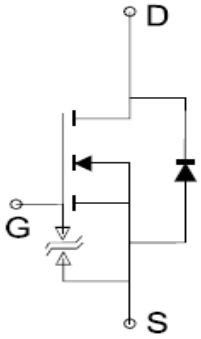
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

PIN CONFIGURATION



DFN1006-3L outline

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain



N-Channel MOSFET

Ordering Information: ME2N7002DN-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.28	A
	T_A=70℃	I_D	0.23	
Pulsed Drain Current		I_{DM}	1.12	A
Maximum Power Dissipation	T_A=25℃	P_D	0.36	W
	T_A=70℃	P_D	0.23	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

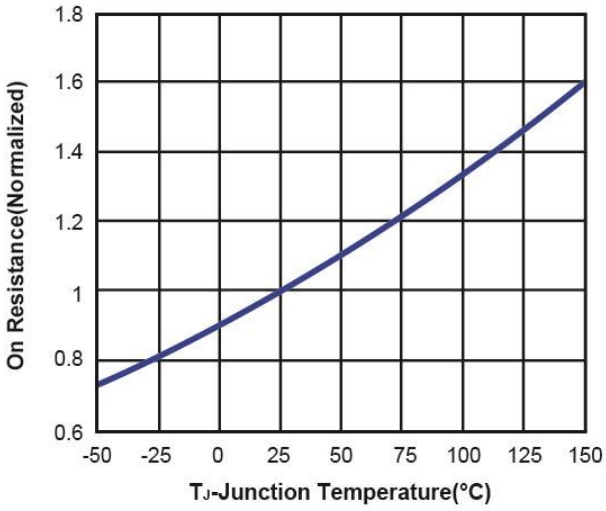
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA		1.75	2.8	Ω
		V_{GS}=4.5V, I_D=200mA		2.2	3.7	
		V_{GS}=3V, I_D=10mA		3.5	4.4	
V_{SD}	Diode Forward Voltage *	I_S=200mA, V_{GS}=0V		0.82	1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=10V,I_D=200mA		3.68		nC
Qg	Total Gate Charge	V_{DS}=30V,V_{GS}=4.5V,I_D=200mA		1.43		
Qgs	Gate-Source Charge			2.1		
Qgd	Gate-Drain Charge			0.28		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		16		pF
Coss	Output Capacitance			2		
Crss	Reverse Transfer Capacitance			1		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, R_L =150Ω V_{GS}=10V,R_G=10Ω I_D=200mA		3.6		ns
t_r	Turn-On Rise Time			23.2		
$t_{d(off)}$	Turn-Off Delay Time			5.5		
t_f	Turn-Off Fall Time			23.2		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

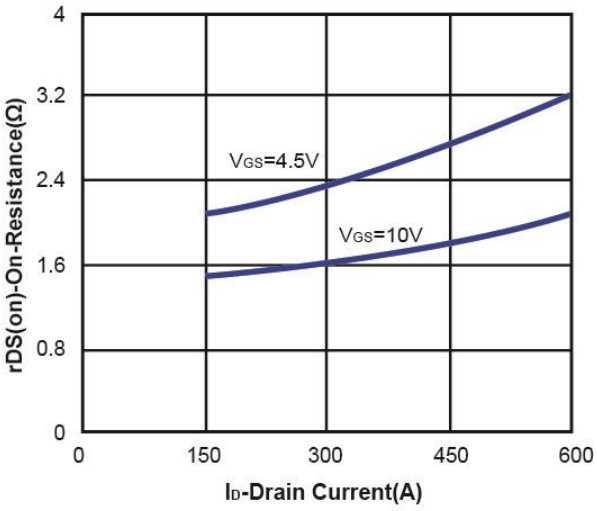
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

Typical Characteristics (T_J =25℃ Noted)

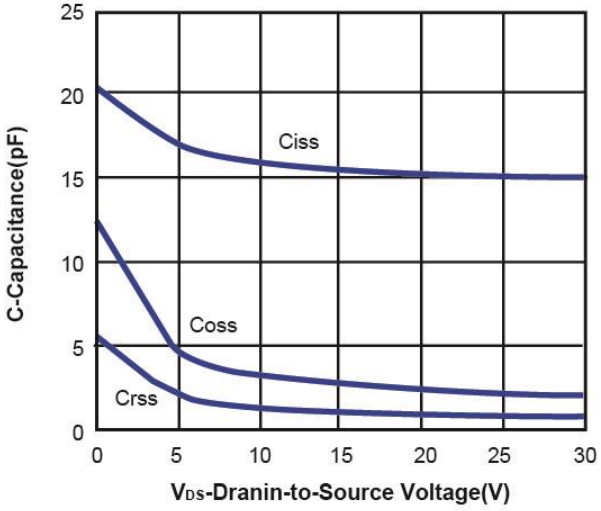
On Resistance vs. Junction Temperature



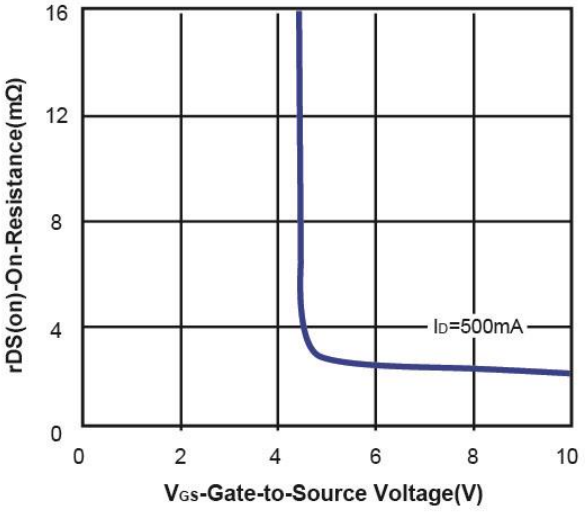
On Resistance vs. Drain Current



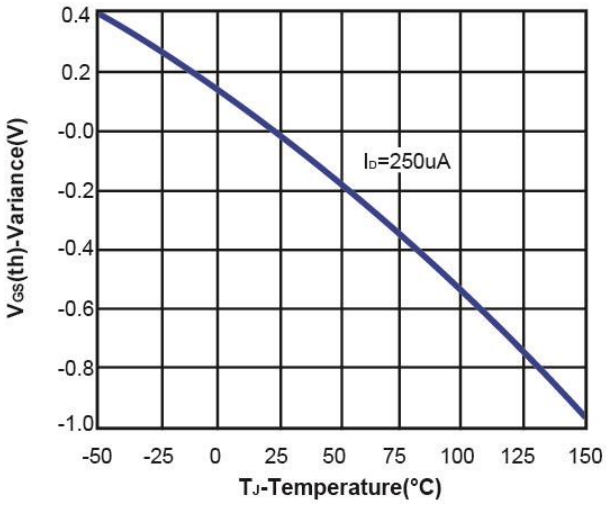
Capacitance



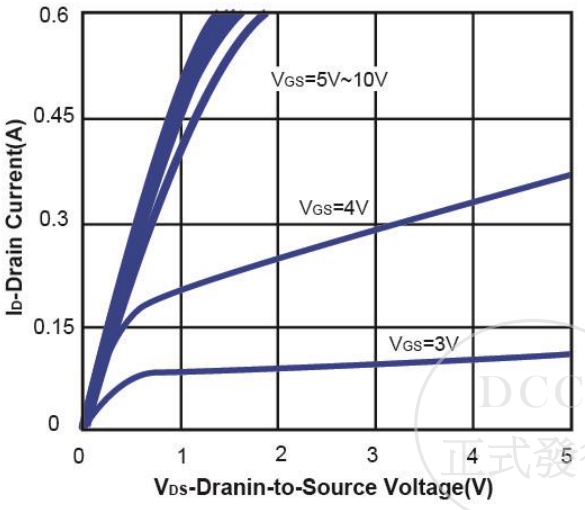
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

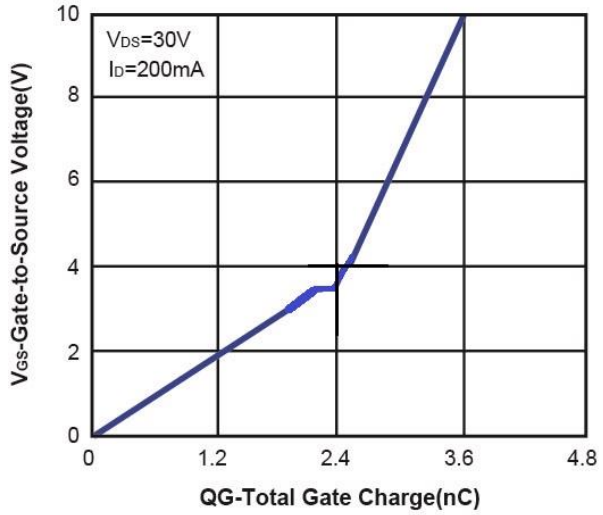


On-Region Characteristics

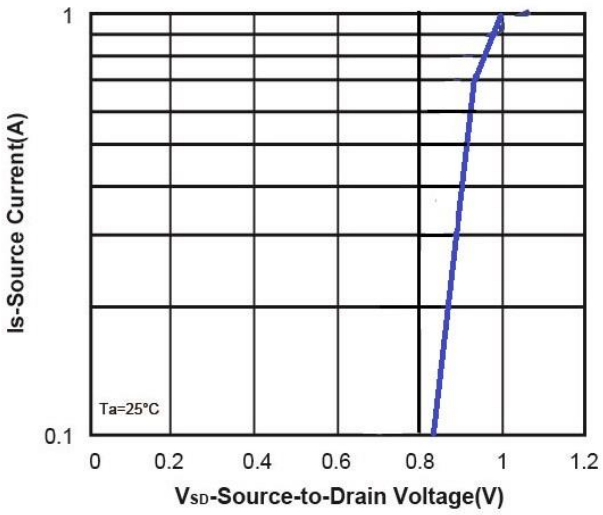


Typical Characteristics (T_J =25℃ Noted)

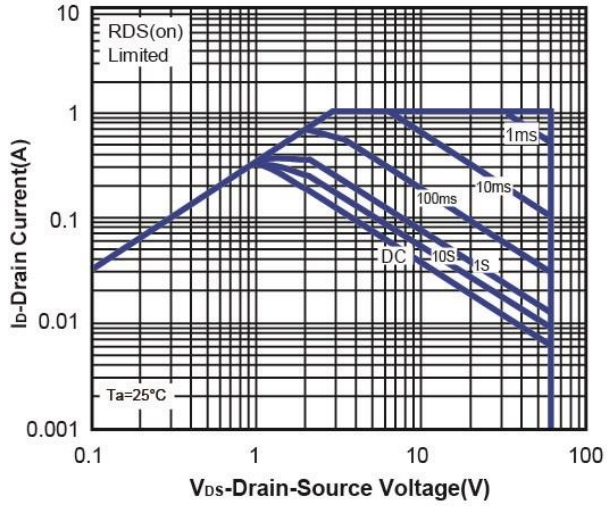
Gate Charge



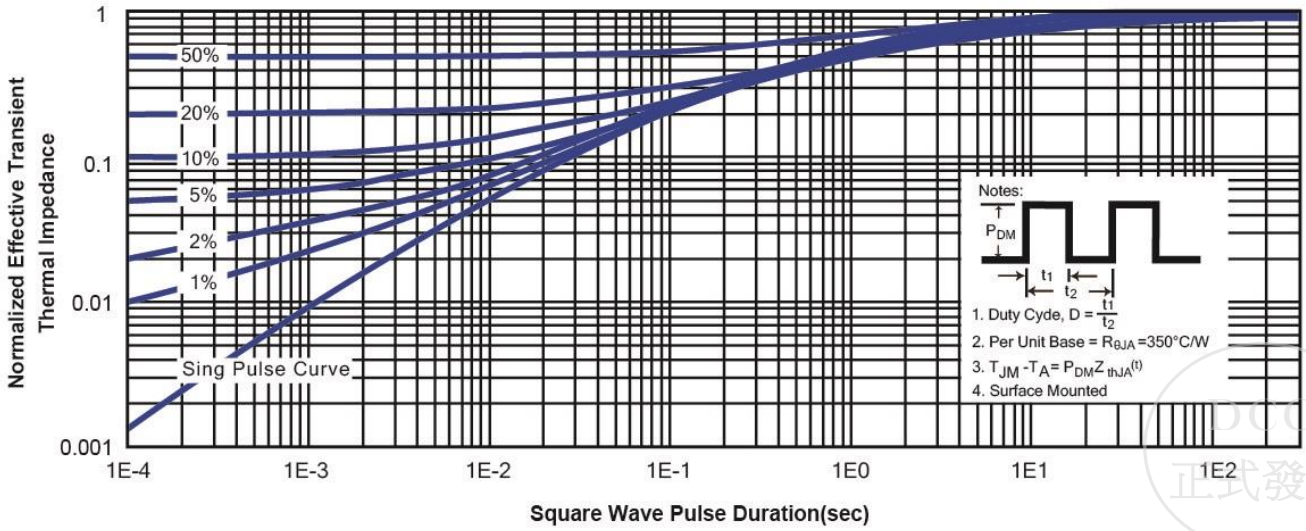
Body-diode characteristics



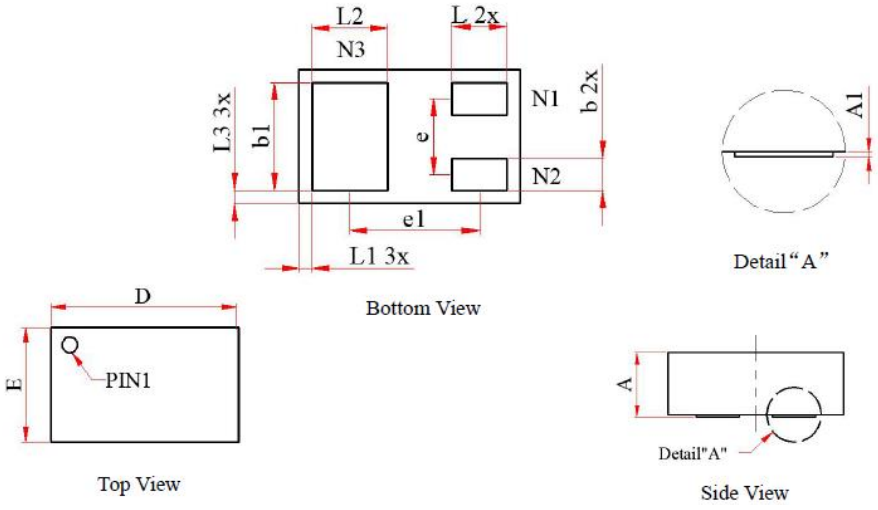
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

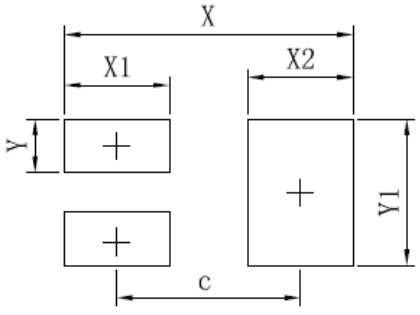


DFN1006-3L Package Outline



Symbol	Dimension In Millimeters		
	Normal	Min	Max
A	--	0.400	0.500
A1	--	--	0.050
D	1.020	0.990	1.050
E	0.620	0.590	0.650
b	0.150	0.100	0.200
b1	0.500	0.450	0.550
L	0.250	0.200	0.300
L1	0.060	0.020	0.100
L2	0.250	0.200	0.300
L3	0.060	0.020	0.100
e	0.350 BSC		
e1	0.650 BSC		

Suggested Pad Layout

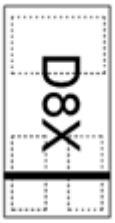


Dimensions	(mm)
C	0.65
X	1.05
X1	0.4
X2	0.4
Y	0.2
Y1	0.55

Device name: ME2N7002DN-G

Package: DFN1006-3L

Marking Code



Top View
Bar Denotes Gate
And Source Side

X:Data Code

MONTH CODE

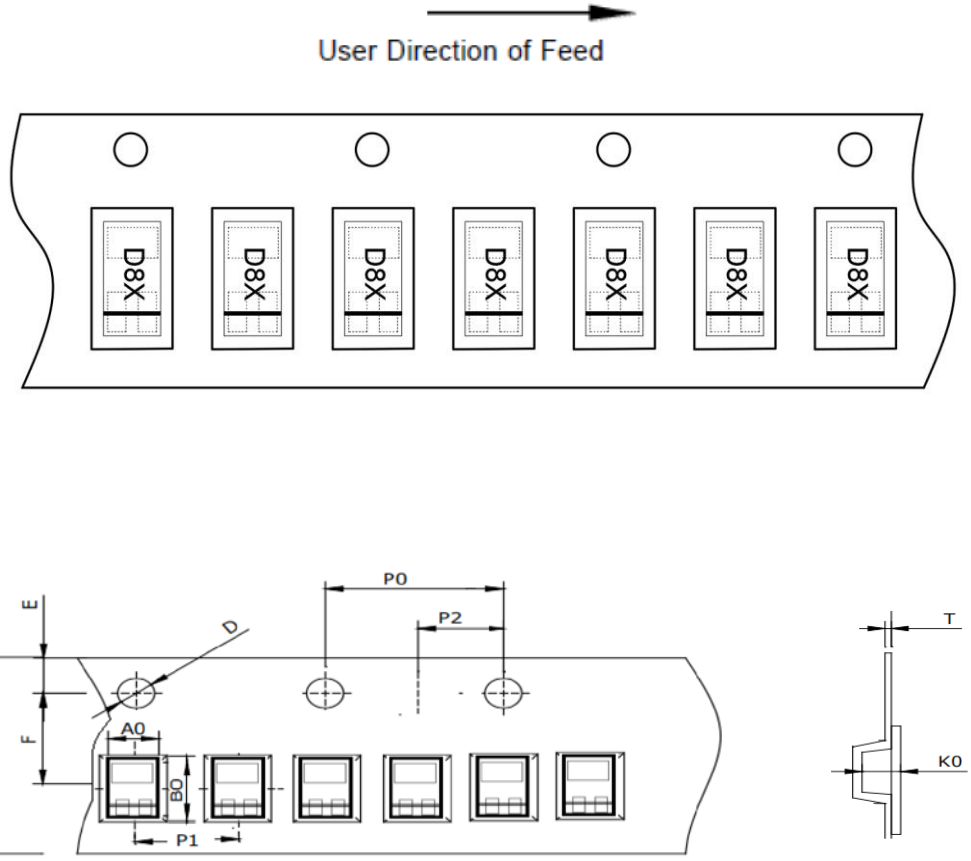
ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

Tape and reel specifications



PACKAGE	W	E	F	P0	D	P2	P1	T	A0	B0	K0
DFN1006-3L	8mm ±0.1	1.75mm ±0.1	3.5mm ±0.05	4mm ±0.1	1.5mm ±0.1	2mm ±0.1	2mm ±0.1	0.23mm ±0.02	0.67mm ±0.05	1.2mm ±0.05	0.55mm ±0.05