

N-Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N7002F is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

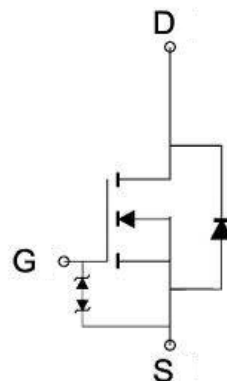
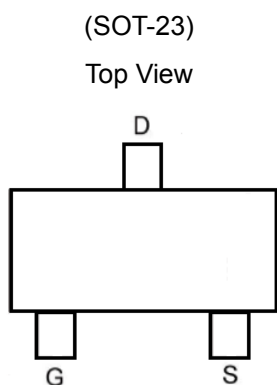
FEATURES

- $R_{DS(ON)} \leq 8\Omega @ V_{GS}=4V$
- $R_{DS(ON)} \leq 13\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information:ME2N7002F (Pb-free)

ME2N7002F-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ C$	0.17
		$T_A=70^\circ C$	0.13
Pulsed Drain Current	I_{DM}	0.7	A
Maximum Power Dissipation	P_D	$T_A=25^\circ C$	0.36
		$T_A=70^\circ C$	0.23
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	350	$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	0.8		1.5	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 10	μA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance ^a	$V_{GS}=4V, I_D=10mA$		5	8	Ω
		$V_{GS}=2.5V, I_D=1mA$		7	13	
V_{SD}	Diode Forward Voltage	$I_S=200mA, V_{GS}=0V$			1.2	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=25V, V_{GS}=10V, I_D=0.22A$		4.9		nC
Q_{gs}	Gate-Source Charge			2.1		
Q_{gd}	Gate-Drain Charge			0.6		
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		21		pf
C_{oss}	Output Capacitance			10		
C_{rss}	Reverse Transfer Capacitance			2		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=5V, R_L=500\ \Omega,$ $V_{GEN}=5V, R_G=10\ \Omega$		10.1		ns
t_r	Turn-On Rise Time			7.3		
$t_{d(off)}$	Turn-Off Delay Time			31.3		
t_f	Turn-Off Fall Time			28.2		

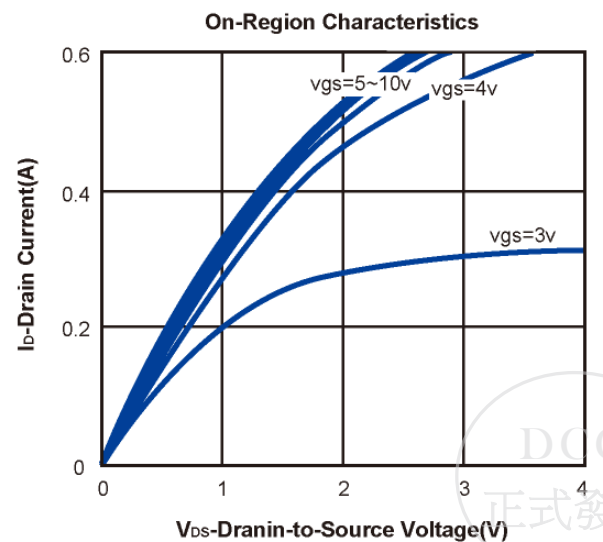
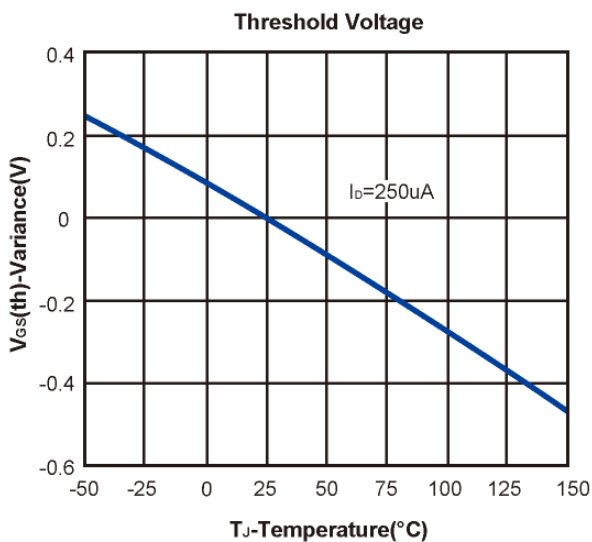
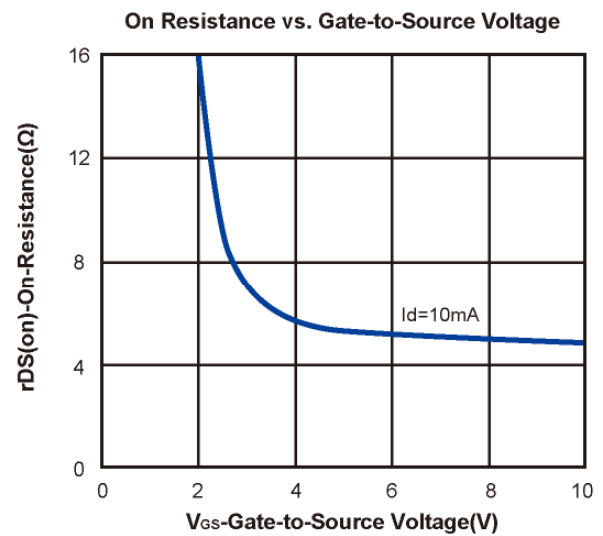
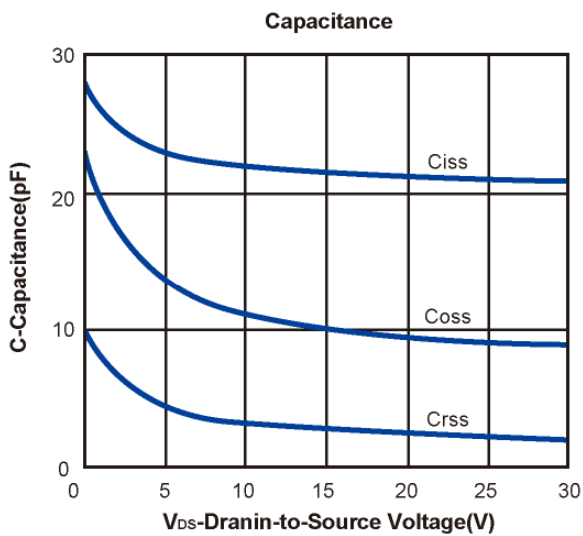
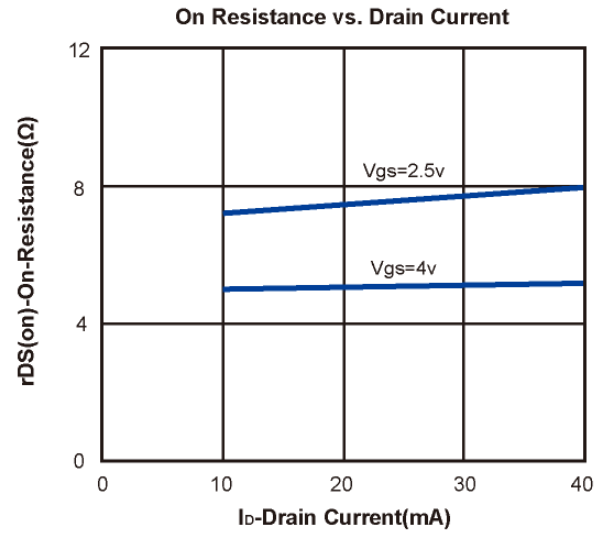
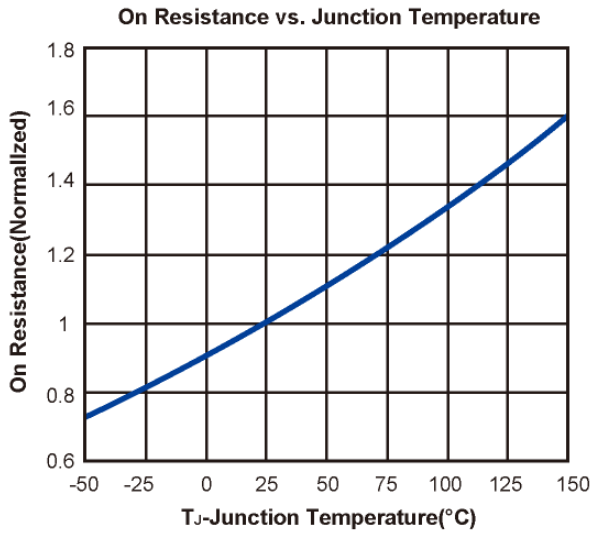
 Notes: a. Pulse test: pulse width $\leq 300\ \mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



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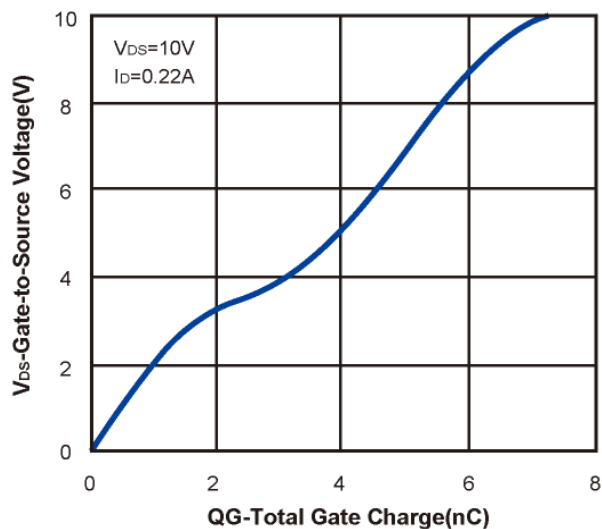
Typical Characteristics (T_J = 25°C Noted)



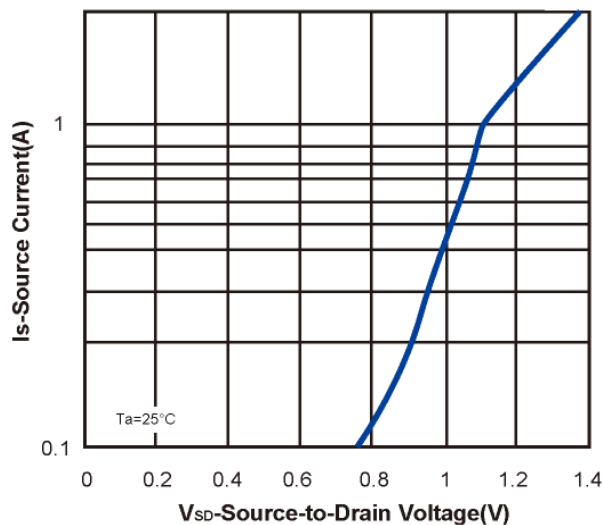
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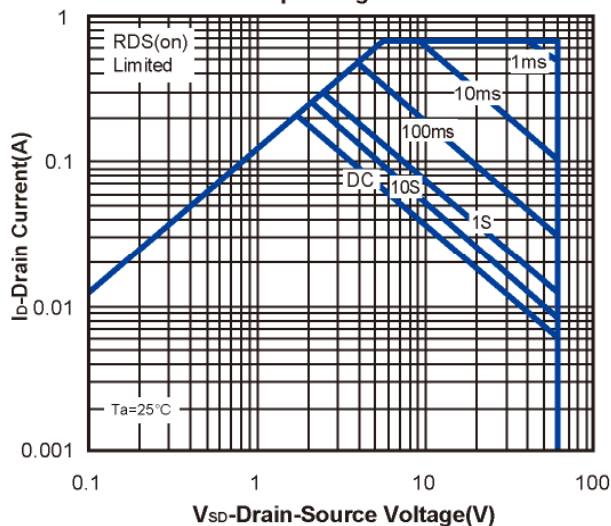
Gate Charge



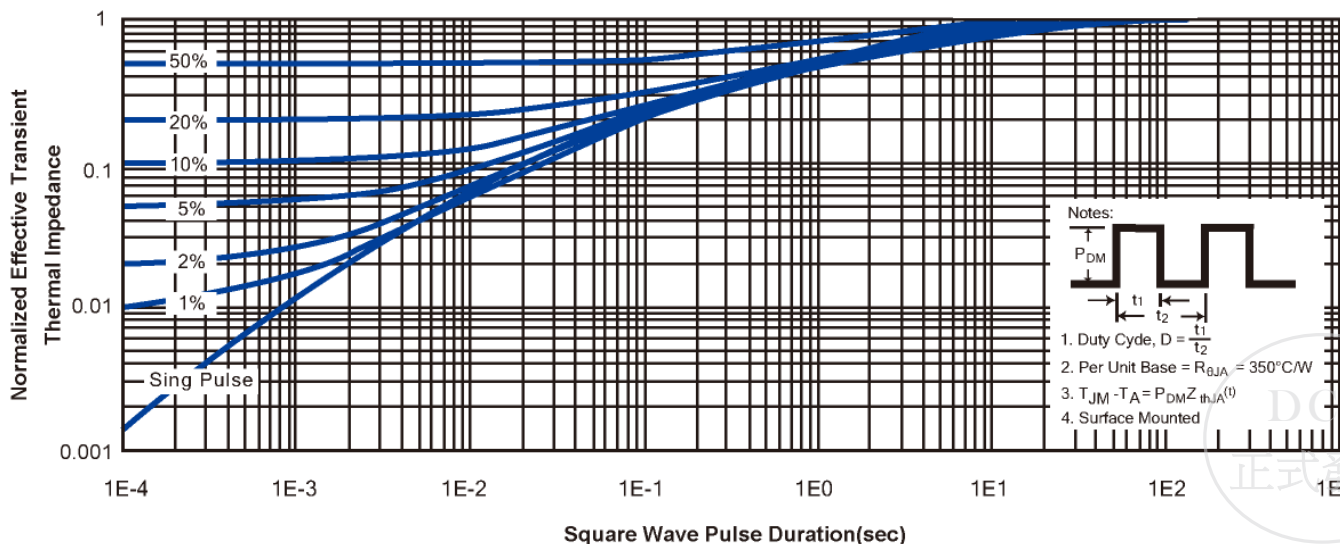
Body-diode characteristics



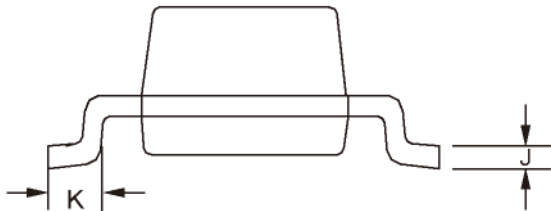
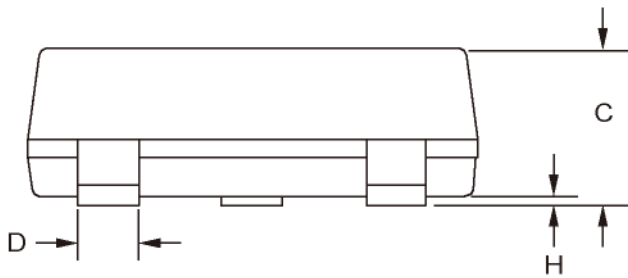
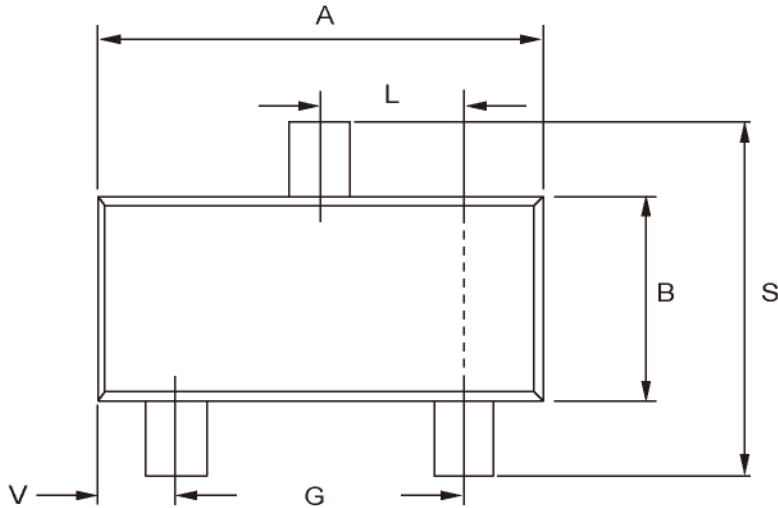
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

