N-Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

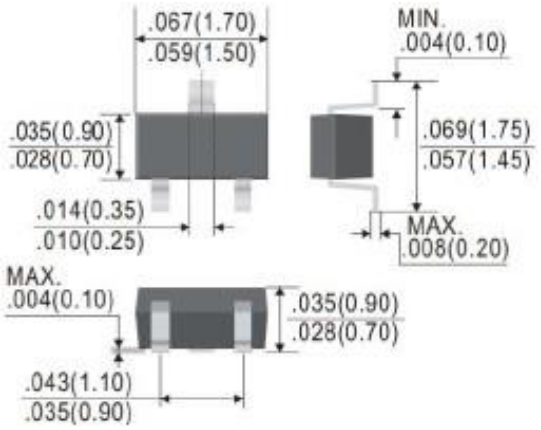
The ME2N7002KWT-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦3Ω@V_{GS}=10V
- $R_{DS(ON)}$ ≦4Ω@V_{GS}=4.5V
- ESD Protected up to 2kV
- Low on resistance RDS(ON)
- Low gate threshold voltage
- Low input capacitance

PIN CONFIGURATION

SOT-523



Ordering Information: ME2N7002KWT-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain	I_D	300	mA
Pulsed Drain Current	I_{DM}	1	A
Maximum Power Dissipation * (Steady State)	P_D	150	mW
Operating Junction Temperature	T_J	- 55 to + 150	℃
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	833	℃/W

* Surface-mounted on FR4 board using 1 in sq pad size

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA			3	Ω
		V_{GS}=4.5V, I_D=200mA			4	
V_{SD}	Diode Forward Voltage	I_S=0.5A, V_{GS}=0V		0.85		V
DYNAMIC						
Qg	Total Gate Charge	V_{GS} =4.5V, V_{DS} =10V, I_D =0.5A		0.44		nC
Qgs	Gate-Source Charge			0.2		
Qgd	Gate-Drain Charge			0.1		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		22.5	50	pF
Coss	Output Capacitance			9	25	
Crss	Reverse Transfer Capacitance			7.5	10	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, V_{GS}=10V, R_G=25Ω, I_D=0.5A		2.7		ns
t_r	Turn-On Rise Time			2.5		
$t_{d(off)}$	Turn-Off Delay Time			13		
t_f	Turn-Off Fall Time			8		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice

Typical Characteristics (T_J =25℃ Noted)

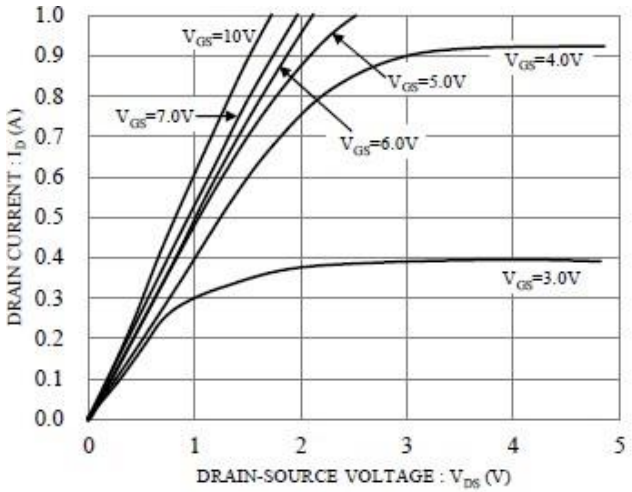


Fig.1 Typical output characteristics

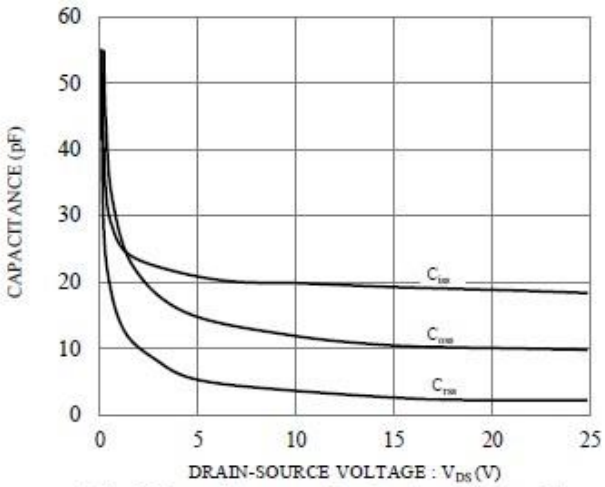


Fig.2 Capacitance vs Drain-to-source voltage

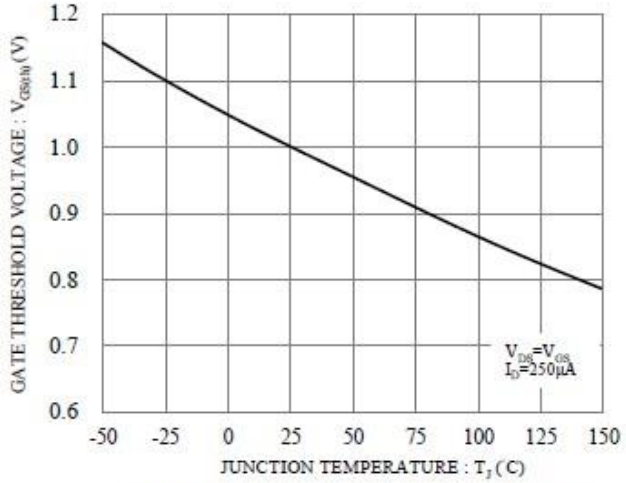


Fig.3 Gate threshold voltage vs. Junction temperature

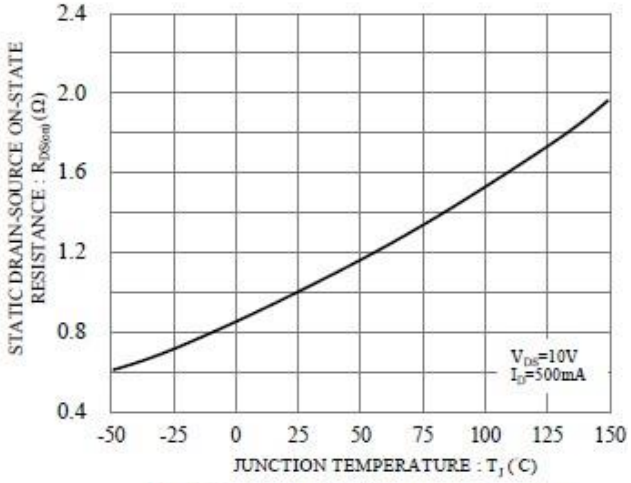


Fig.4 On-State Resistancevs. Junction temperature

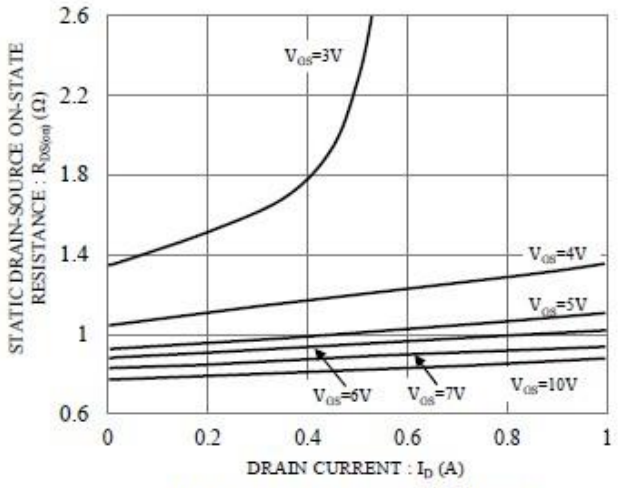


Fig.5 Static drain-source on-state resistance vs. Drain current

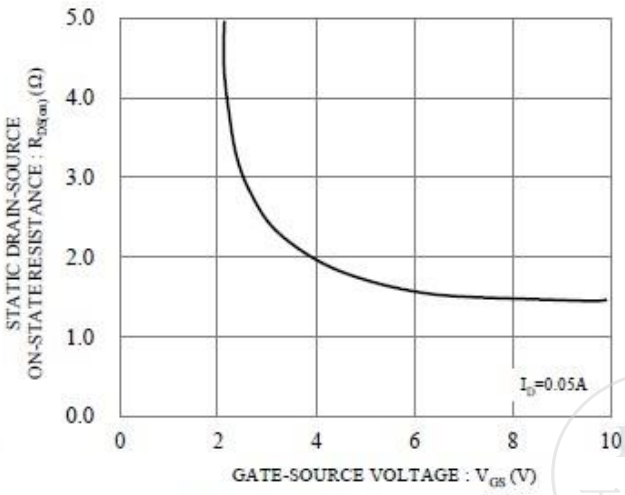
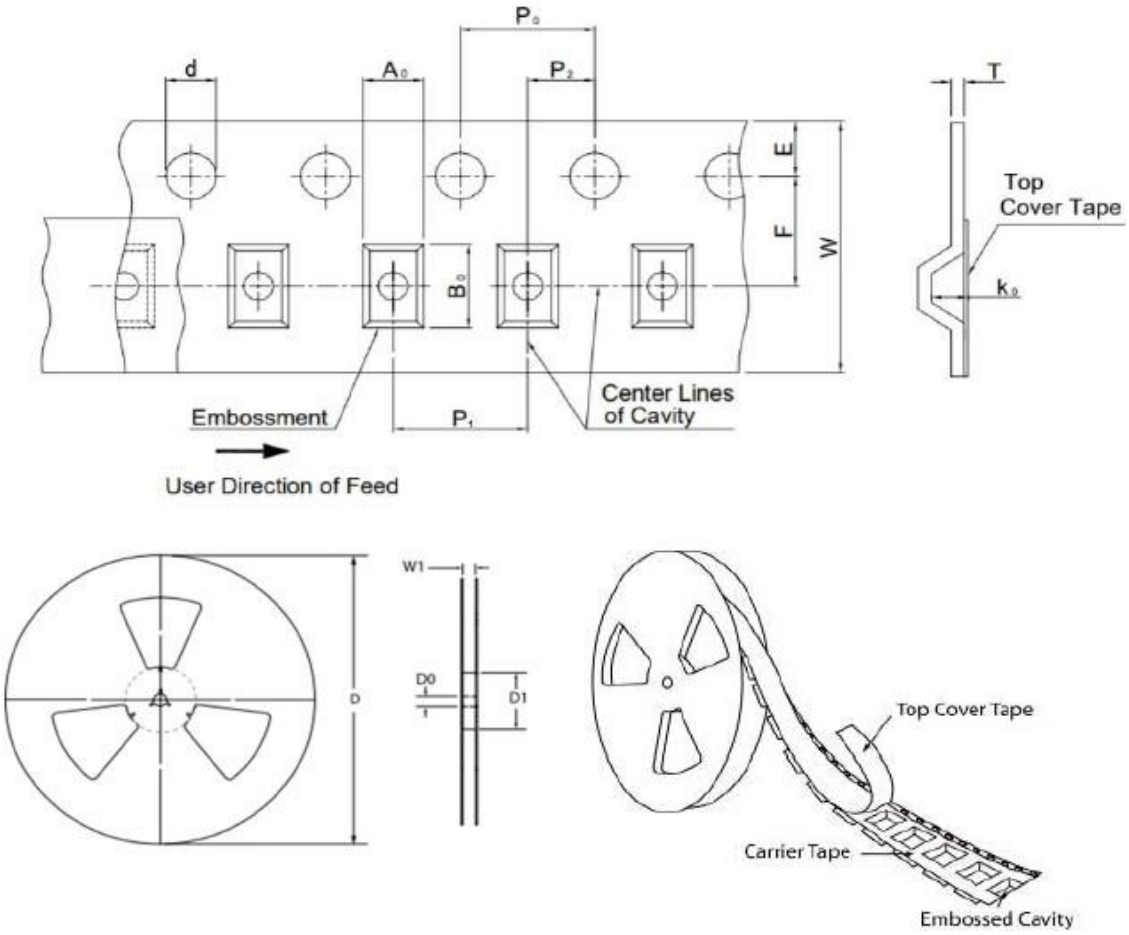


Fig.6 Static drain-source on-state resistance vs. Gate-source voltage

TAPE & REEL SPECIFICATION



Item	Symbol	SOT-523
Carrier width	A_0	1.90 ± 0.10
Carrier length	B_0	1.95 ± 0.10
Carrier depth	K_0	1.10 ± 0.10
Sprocket hole	d	1.50 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D_0	13.00 ± 0.50
Reel inner diameter	D_1	MIN. 50.00
Sprocke hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocke hole pitch	P_0	4.00 ± 0.10
Punch hole pitch	P_1	4.00 ± 0.10
Embossment center	P_2	2.00 ± 0.10
Overall tape thickness	T	MAX. 0.60
Tape width	W	8.00 ± 0.30
Reel width	W1	MAX. 10.00

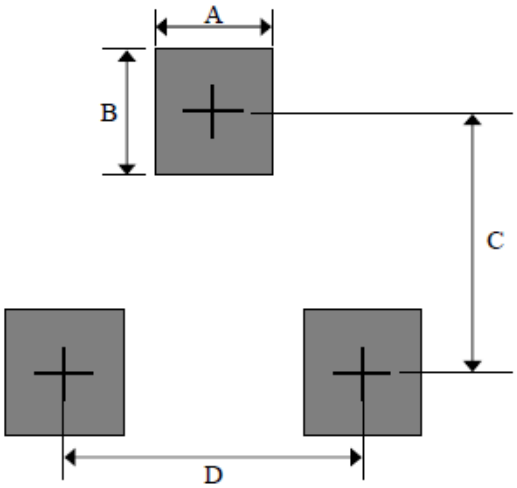
ORDER INFORMATION

Package	Reel Size	Quantity
SOT-523	7"	4,000

ORDER INFORMATION

Part Number	Marking Code
ME2N7002KWT-G	MP

SUGGESTED SOLDER PAD LAYOUT



Unit : mm

PACKAGE	A	B	C	D
SOT-523	0.70	0.70	1.30	1.00