

P-Channel 30V (D-S) MOSFET

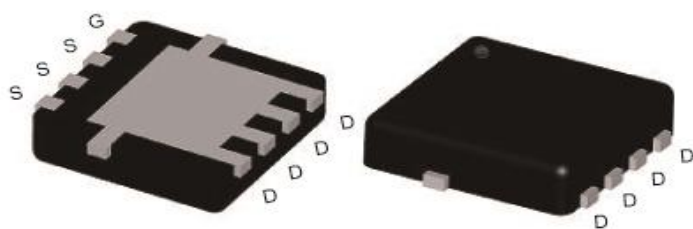
GENERAL DESCRIPTION

The ME7807S is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(DFN(S) 3X3)

Top View

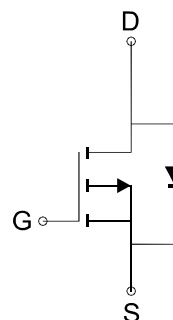


FEATURES

- $R_{DS(ON)} \leq 15m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 29.5m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC



P-Channel MOSFET

Ordering Information: ME7807S (Pb-free)

ME7807S-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	-29	A
	$T_C = 70^\circ C$		-23	
Single pulse Avalanche Energy $L = 0.1mH$	$T_C = 25^\circ C$	I_{AS}	25	A
Single pulse Avalanche Energy $L = 0.1mH$	$T_C = 25^\circ C$	E_{AS}	31.2	mJ
Pulsed Drain Current		I_{DM}	-88	A
Maximum Power Dissipation	$T_C = 25^\circ C$	P_D	25	W
	$T_C = 70^\circ C$		16	
Operating Junction Temperature		T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case *		$R_{\theta Jc}$	5	$^\circ C/W$

* The device mounted on $1in^2$ FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1.3		-2.3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-10V, I _D = -12A		11	15	mΩ
		V _{GS} =-4.5V, I _D = -10A		20	29.5	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V			-1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-8A		33.8		nC
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-8A		14.7		
Q _{gs}	Gate-Source Charge			9		
Q _{gd}	Gate-Drain Charge			10.6		
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		1380		pF
C _{oss}	Output Capacitance			221		
C _{rss}	Reverse Transfer Capacitance			208		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =3Ω I _D =-5A, V _{GEN} =-10V R _G =3Ω		17.6		ns
t _r	Turn-On Rise Time			44.9		
t _{d(off)}	Turn-Off Delay Time			60		
t _f	Turn-On Fall Time			34.5		

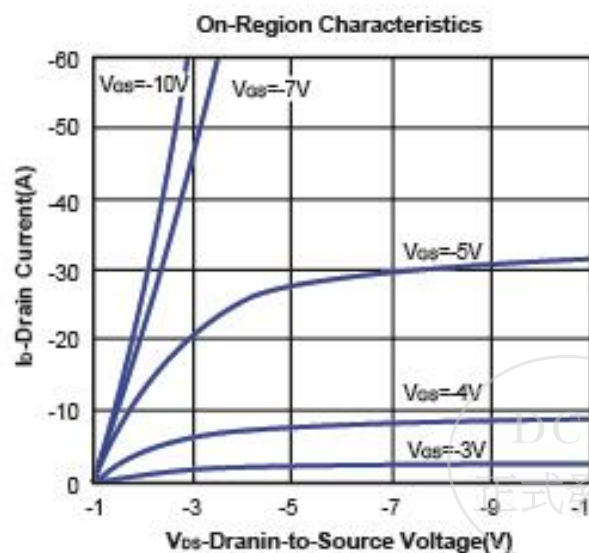
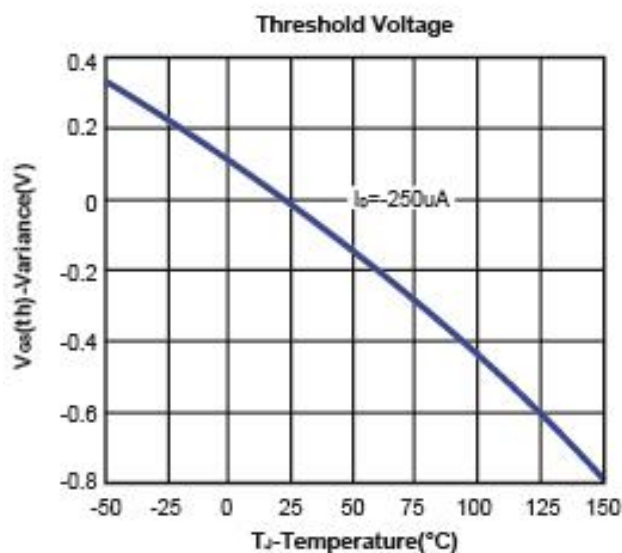
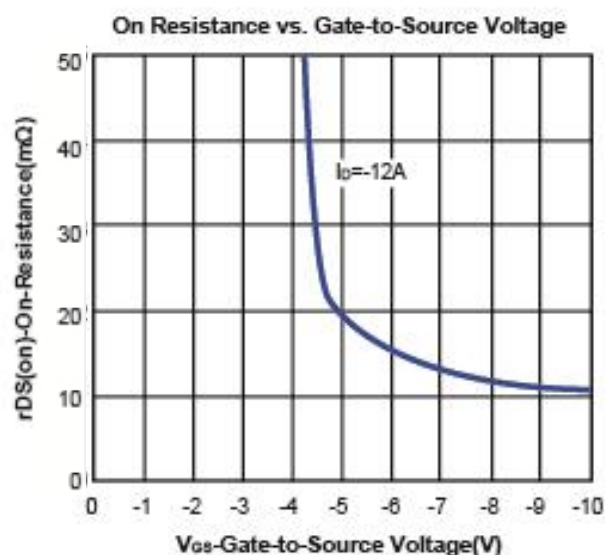
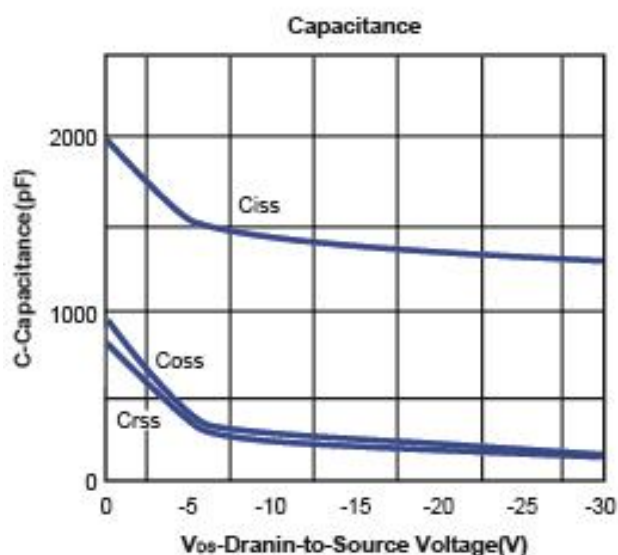
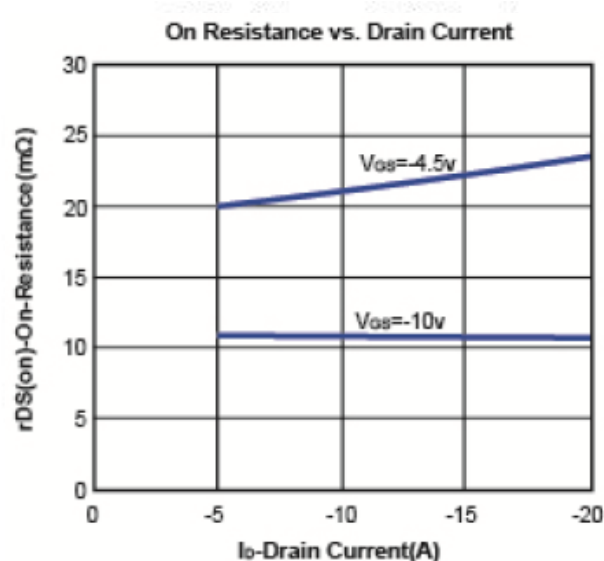
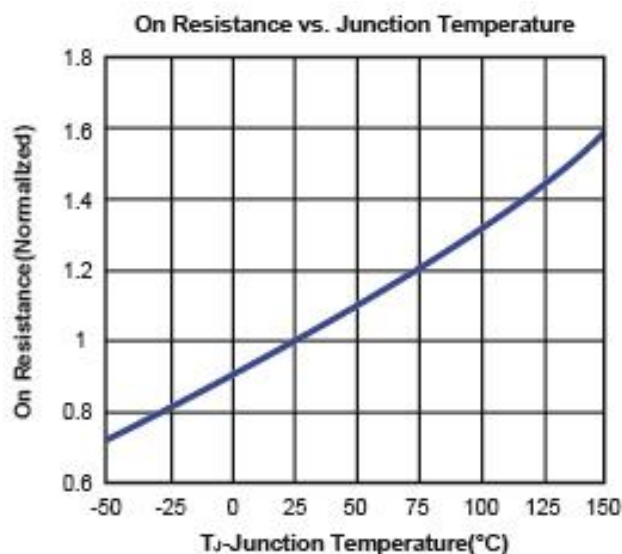
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions , reliability, qualified manufacturer without notice.

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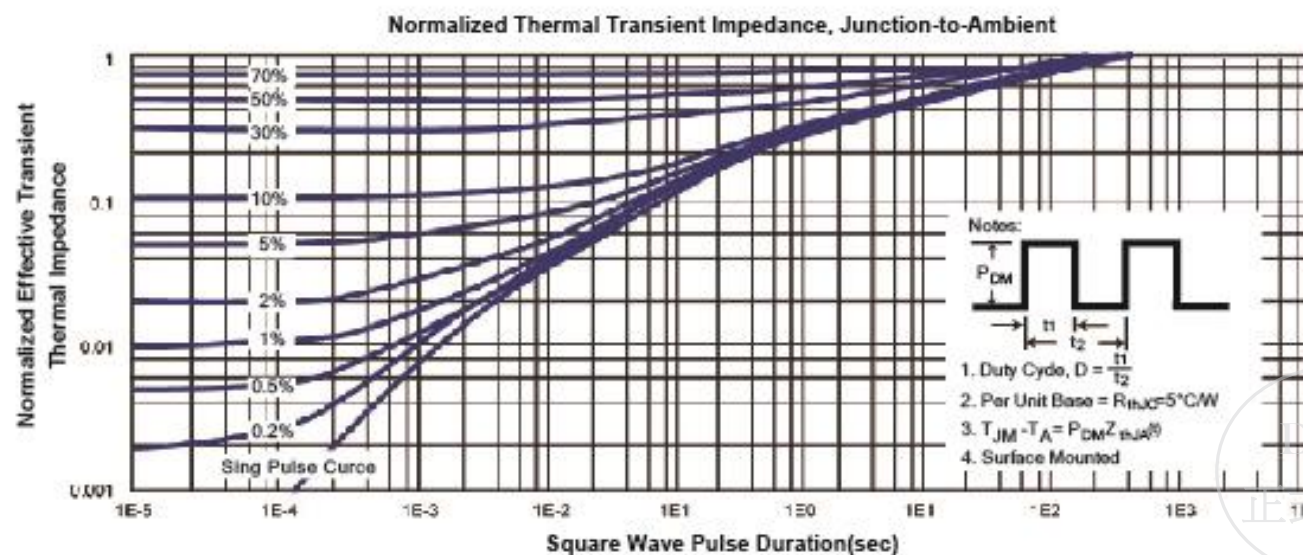
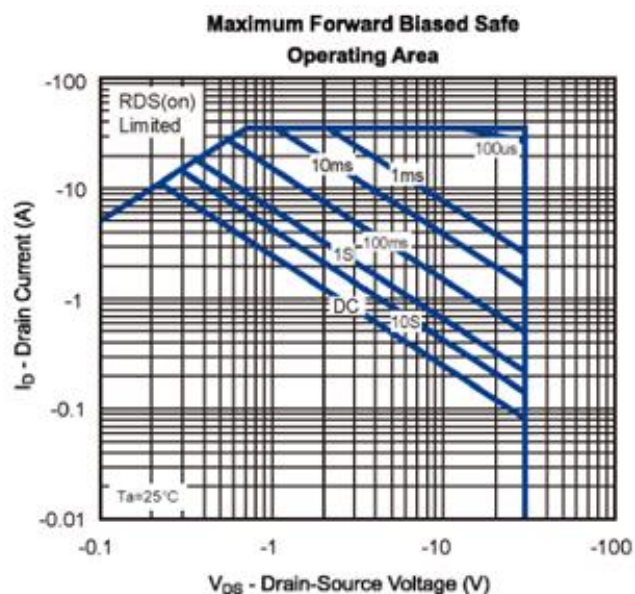
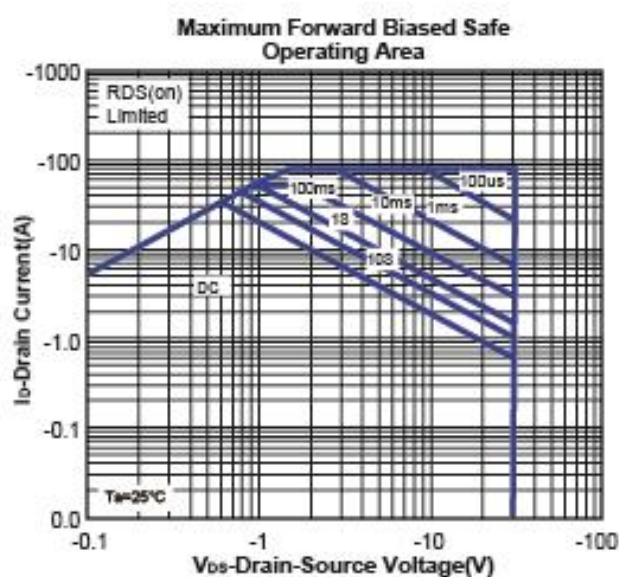
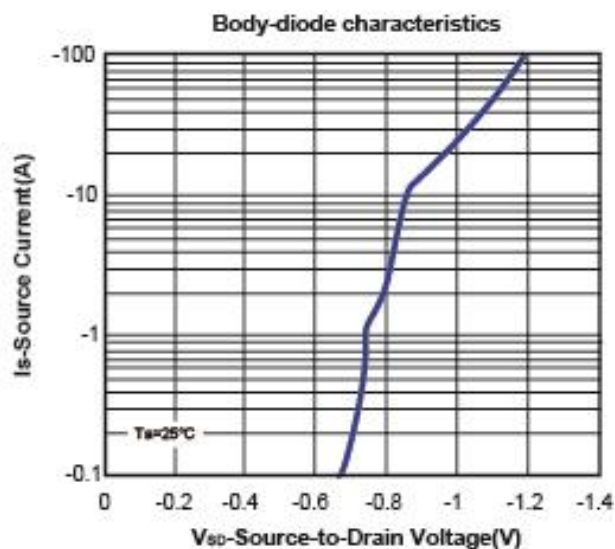
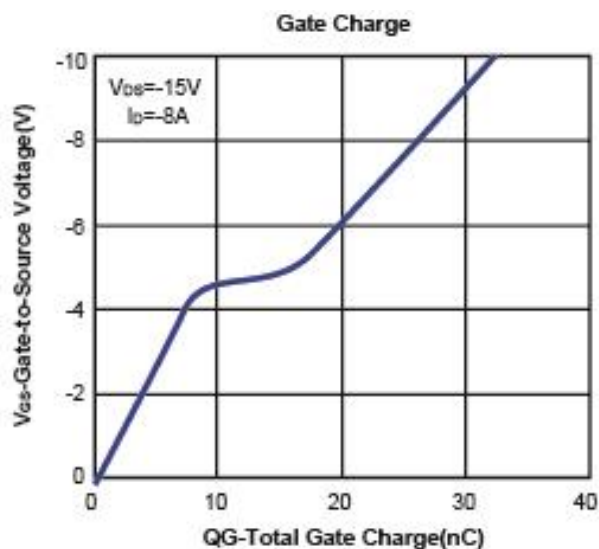
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Typical Characteristics (T_J = 25°C Noted)

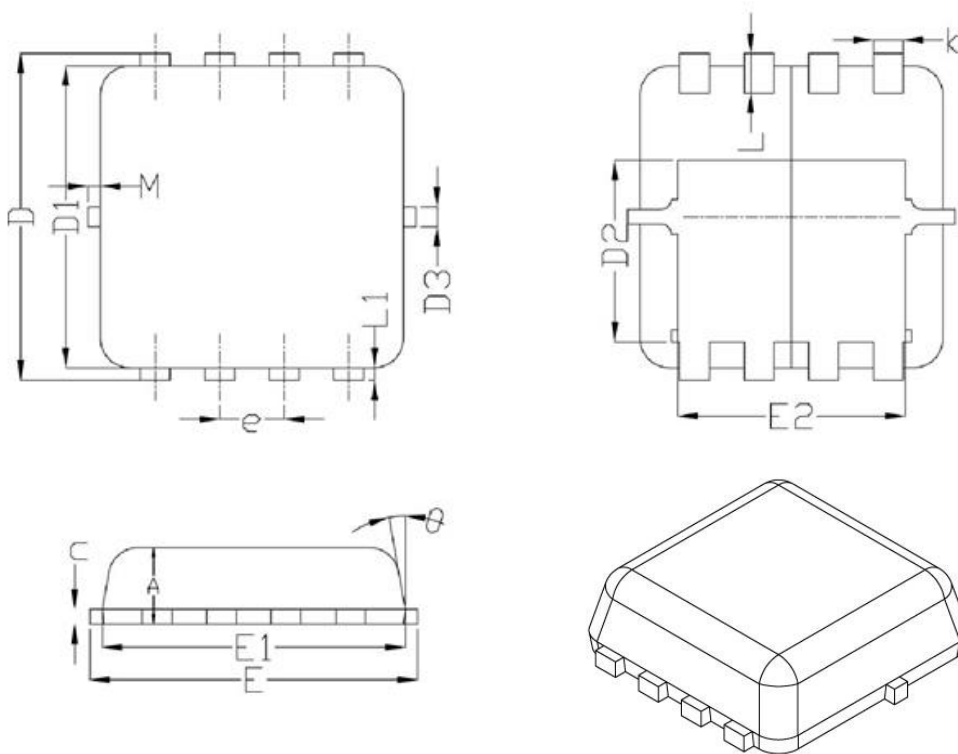


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Typical Characteristics (T_J = 25°C Noted)



DFN(S)3X3 Package Outline



SYMBOL	DIMENSIONAL REQMTS	
	MIN	MAX
A	0.70	0.90
b	0.20	0.40
c	0.08	0.25
D	2.70	3.45
D1	2.20	3.20
D2	1.54	1.98
D3	0.10	0.30
E	3.15	3.45
E1	2.80	3.30
E2	2.25	2.65
e	0.65BSC	
H	0.28	0.68
L	0.30	0.50
L1	0.06	0.20
θ	---	12°
M	*	0.15
* Not specified		

